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THESIS

FIELD PROGRAMMABLE GATE ARRAY HYSTERESIS CONTROL OF PARALLEL CONNECTED INVERTERS

by

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June 2006

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13. ABSTRACT (maximum 200 words)

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FIELD PROGRAMMABLE GATE ARRAY HYSTERESIS CONTROL OF PARALLEL CONNECTED INVERTERS

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ABSTRACT

This thesis presents the use of a Field Programmable Gate Array (FPGA) to control two Commercial-Off-The-Shelf (COTS) Power Electronic Building Blocks (PEBB) configured to produce a three-phase low distortion sine wave output. The next generation warship is expected to contain more electric loads that require quality variable frequency output. A typical propulsion motor in the 40MW range will probably require the current Total Harmonic Distortion to be less than 3% (MIL-STD-1399). However, high power low distortion inverters usually have associated high cost and weight penalties. This thesis presents a parallel hybrid converter which demonstrates the use of a high power low fidelity bulk inverter with a low power high fidelity active filter. The high power low fidelity output is sourced using a six-step inverter which produces the entire fundamental current. The low power hysteresis controlled active filter section produces only cancelling harmonic current. The paralleled result is a pristine output sine wave with a 1% current Total Harmonic Distortion (THD). This solution should offer the Navy a high fidelity high power inverter without the cost and weight penalties.

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LIST OF SYMBOLS, ACRONYMS, AND ABBREVIATIONS

A	Amps
AC	Alternating Current
A/D	Analog to Digital Converter
BNC	Bayonet Nut Connector
BOM	Bill of Materials
CPLD	Complex Programmable Logic Device
COTS	Commercial-Off-The-Shelf
CSI	Current-Source Inverter
D/A	Digital to Analog Converter
dB	Decibel
DC	Direct Current
DC-AC	Direct Current to Alternating Current
dv/dt	Derivative of voltage with respect to time
FPGA	Field Programmable Gate Array
GIC	Generalized Impedance Converter
GTO	Gate-Turn-Off Transistors
HDL	Hardware Description Language
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IPS	Integrated Power System
ISP	Indexed Sequential Processor
JTAG	Joint Test Action Group *developer of IEEE Standard 1149.1-1990*
kVA	Kilo Volt Amps
KVL	Kirchhoff's Voltage Law
L	Inductance
MOSFET	Metal-Oxide-Silicon Field Effect Transistor
MTBF	Mean Time Between Failure
MW	Mega Watts
NAVSEA	Naval Sea Systems Command

NPS	Naval Post Graduate School
NRAC	Naval Research Advisory Committee
ns	Nanosecond
ONR	Office of Naval Research
PCB	Printed Circuit Board
PCHI	Parallel Connected Hybrid Inverters
PEBB	Power Electronics Building Blocks
PETS	Power Electronics Teaching System
PROM	Programmable Read-Only Memory
PWM	Pulse Width Modulation
R	Resistance
RMS	Root Mean Square
SR	Set Reset
THD	Total Harmonic Distortion
V	Volts
V_{DC}	Volts Direct Current
VSI	Voltage-Source Inverter
Z	Impedance

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EXECUTIVE SUMMARY

As naval technology continues to advance, the power electronic systems installed in ships must become more efficient, versatile and dependable. Innovation in methods to supply quality power to shipboard war fighting systems will provide the key to creating a modern and capable fleet.

The quality of power is measured by the amount of Total Harmonic Distortion (THD) of the current and voltage present at the load. The Navy limit for THD depends on application; however the most restrictive limit for current THD is less than 3%. The IEEE recommends a current THD limit of less than 2.5% on any single user system such as a ship.

Quality power is important because many alternating current electrical loads are designed to interface with harmonic free sources. For instance, motors perform a multitude of critical functions aboard naval ships; in order to reduce torque pulsations, transmitted noise and extend motor life, current THD and voltage transients (dv/dt) must be kept to a minimum. A hybrid inverter that combines a robust rugged bulk inverter with an active filter is one possible way of providing power that meets the Navy's requirements. This thesis intends to demonstrate the feasibility of one type of parallel hybrid system.

A hybrid inverter system is one that utilizes a bulk inverter for most or all of the real power in conjunction with a second inverter that actively filters to achieve the desired wave form. These types of topologies are candidates to convert DC to the AC necessary to power a motor in the 40MW range. The hybrid system investigated in this thesis consists of a bulk six-step three-phase Voltage-Source Inverter (VSI) and a high-fidelity hysteresis controlled Current-Source Inverter (CSI). The goals of this thesis are as follows:

- Create a SIMULINK® model in order to determine the feasibility of the parallel hybrid concept.

- Construct a custom printed circuit card to interface a Field Programmable Gate Array (FPGA) controller with two Power Electronic Building Blocks (PEBB) that form the high voltage section.
- Use the SIMULINK® model, the constructed interface circuit card, the FPGA controller, and two Commercial-Off-The-Shelf (COTS) PEBBs to implement the parallel hybrid system in hardware.

In order to achieve the goals of this thesis a model was constructed using SIMULINK® blocks for all the components of the system including a VSI PEBB, a CSI PEBB, a wye connected load, an NPS custom interface card and an FPGA controller. The model demonstrated proof-of-concept and potential hardware performance.

An interface card was designed, built and tested. The NPS card allows the XILINX® Virtex-II^{TM} FPGA development kit to be interfaced with the two COTS PEBBs. The XILINX® FPGA allows the SIMULINK® model to be loaded into the FPGA.

The parallel hybrid system hardware components were assembled and the FPGA controller was programmed. An iterative process was used to validate the models with experimental results obtained with actual hardware.

The model and theory predicted that the THD would be less than 1% for the line-to-neutral current wave form. This was confirmed via experimentation.

Successful testing of the controller has validated the efficacy of the system for potential use with large future naval propulsion motors. Laboratory results showed that the hysteresis controlled active filter is capable of reducing the THD to less than 1%, well below the Navy and IEEE standards.

I. INTRODUCTION

As naval technology continues to advance, the power electronic systems installed in ships must become more efficient, versatile and dependable. Innovation in methods to supply clean power to shipboard war fighting systems will provide the key to creating a modern and capable fleet.

The quality of power is measured by the amount of Total Harmonic Distortion (THD) of the current and voltage present at the load. The Navy limit for THD depends on application; however the most restrictive limit for current THD is less than 3% [1]. The IEEE recommends a current THD limit of less than 2.5% on any single user system such as a ship. [2].

A. INTEGRATED POWER SYSTEMS

In January 2000, the Secretary of the Navy selected electric drive to propel all future classes of Naval warships. He stated that, "Changes in propulsion systems fundamentally change the character and the power of our forces. This has been shown by the movement from sails to steam or from propeller to jet engines… More importantly, electric drive, like other propulsion changes, will open immense opportunities for redesigning ship architecture, reducing manpower, improving ship life, reducing vulnerability and allocating a great deal more power to war-fighting applications" [3]. The next generation combatant warship will be constructed using an Integrated Power System (IPS) to unlock propulsion power and enable these "immense opportunities".

The benefits of using an IPS system are [4, 5]:

- Signature Reduction: Less prime mover machinery equates to reduced infrared and acoustic signatures.
- Fuel Savings: There is an anticipated 15-20% savings in fuel consumption over the life of the ship. A smaller propulsion plant is required to produce greater available power. Only the power generators needed to match the ship's load requirements will be online.
- Economical Construction: Ship construction costs are reduced due to the modular nature of the IPS architecture. Additionally, the modular design allows for quicker repair and modernization over the life of the ship.

Reduced ship's displacement equates to a higher maximum speed or greater payload capacity.

- Reduced Life-Cycle Costs (up to 50%): Longer Mean Time Between Failures (MTBF) of propulsion system components means less manpower is required to maintain the machinery. There is a 50% reduction in engine maintenance when compared to existing ships.
- Increased Survivability: Shorter electric motor drive and shafting as compared to mechanical drive propulsion motors and shafting allows for increased propulsion system compartmentalization, resulting in increased ship survivability.
- Enabler for Tomorrow's Weapons: Unlocking propulsion power and allowing it to be used for the next generation pulsed and high power weapons systems is possible due to increased load sharing between all shipboard systems.

A fundamental key to the success of the IPS is the ability to deliver quality power. An efficient clean method of converting from DC to AC power is needed. Quality power is important because many alternating current electrical loads are designed to interface with harmonic free sources. For instance, motors perform a multitude of critical functions aboard naval ships; in order to reduce torque pulsations, transmitted noise and extend motor life, current THD and voltage transients (dv/dt) must be kept to a minimum. A hybrid inverter that combines a robust rugged bulk inverter with an active filter is one possible way of providing power that meets the Navy's requirements. This thesis intends to demonstrate the feasibility of one type of parallel hybrid system.

B. RESEARCH GOALS

This thesis will continue the research conducted by previous students on the hybrid inverter systems [6]. A hybrid inverter system is one that utilizes a bulk inverter for most or all of the real power in conjunction with a second inverter that actively filters to achieve the desired wave form. These types of topologies are candidates to convert DC to the AC necessary to power a motor in the 40MW range. The hybrid system investigated in this thesis consists of a bulk six-step three-phase Voltage-Source Inverter (VSI) and a high-fidelity hysteresis controlled Current-Source Inverter (CSI). The goals of this thesis are as follows:

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Successful testing of the controller will validate the efficacy of the system for potential use with large future naval propulsion motors.

C. APPROACH

A mathematical model of the bulk inverter, hysteresis inverter, load and control circuitry was created in MATLAB® using the SIMULINK® modeling tool. Two 20kVA SEMIKRON Isolated Gate Bipolar Transistor (IGBT) based COTS PEBB inverters were purchased. The PEBBs each have three parallel connected half-bridges rated at 50A, 1200V and an IGBT-diode brake for protection. A MEMEC^{TM} development kit containing a XILINX® FPGA was purchased and the NPS custom interface card constructed. The NPS custom card includes output control for the bulk inverter and the hysteresis or conditioning inverter. The custom card also includes a 4-channel Analog-to-Digital (A/D) converter used to detect load currents and provide feedback. The FPGA was programmed with the model created in SIMULINK® and used to drive both the bulk and hysteresis PEBBs. The output current wave forms were well within the Navy's THD limits. Finally, the results were measured and compared to computer simulations.

D. THESIS ORGANIZATION

Chapter I is an overview of the research effort and the layout of the thesis.

Chapter II contains a definition of THD, a concept H-bridge inverter, a description of a six-step three-phase inverter, explanation of a hysteresis controlled inverter, a depiction of a PEBB, and a overview of an FPGA.

Chapter III presents the computer model and the simulation results.

Chapter IV contains the design, testing and construction the NPS custom FPGA interface card.

Chapter V chronicles the experimental results from the lab built prototype.

Chapter VI provides conclusions and future research opportunities.

Appendix A contains pertinent computer code and SIMULINK® models. Appendix B contains relevant circuit schematics and netlist for the NPS interface card. Appendix C provides information concerning the SEMIKRON PEBBs and MEMC FPGA development kit.

II. BACKGROUND INFORMATION

A. OVERVIEW

This chapter provides basic background information necessary for the understanding of the parallel hybrid inverter explored in this thesis. Thus, chapter II contains a definition of THD, a concept H-bridge inverter, a description of a six-step three-phase inverter, explanation of a hysteresis controlled inverter, a depiction of a PEBB, and a overview of an FPGA.

B. TOTAL HARMONIC DISTORTION

THD is a measure of the degree to which a sinusoidal wave shape is distorted by harmonic wave forms and usually expressed as a percentage. The higher value of the THD the greater the deviation is from a sine wave. A perfect sine wave will have a THD equal to 0%. The mathematical formula for current $\mathrm{THD_i}$ can be written as

$$\mathrm{THD_i} = 100 \times \sqrt{\sum_{k=2,3,4\ldots}^{\infty} \frac{\left(I_k\right)^2}{\left(I_1\right)^2}} \tag{2.1}$$

where *k* is the integer order of the harmonic and I_k is the magnitude of k^{th} harmonic. A similar index $\mathrm{THD_v}$ can be expressed by using voltage components.

Torque pulsations can be caused by using less than poly-phase power or through the use of non-sinusoidal voltage to drive motors [7]. Torque pulsations will have the undesirable effects of speed fluctuations, vibration noise and wasted energy. In order to reduce unwanted torque pulsations the Navy uses poly-phase power for its motors and sets an upper limit on THD.

Consider the square wave with amplitude 1 and a frequency of ω given by the function sq(ωt).

$$\mathrm{sq}(\omega t) = \mathrm{sgn}\left(\cos(\omega t)\right) \text{ where } \mathrm{sng}(x) = \begin{cases} 1 & x > 0 \\ 0 & x = 0 \\ -1 & x < 0 \end{cases} \tag{2.2}$$

The sq(ωt) function will exhibit a period of T=2π/ω. The average value of sq(ωt) is zero and the RMS value is one. The fundamental and harmonics can be computed by evaluating the Fourier series. Let ωt =θ then the Fourier series coefficients a_n and b_n are:

$$\begin{aligned} a_n &= \frac{1}{\pi}\int_{-\pi/2}^{3\pi/2} \mathrm{sq}(\theta)\cos(n\theta)\,d\theta \\ &= \frac{1}{\pi}\int_{-\pi/2}^{\pi/2} \cos(n\theta)\,d\theta - \frac{1}{\pi}\int_{\pi/2}^{3\pi/2} \cos(n\theta)\,d\theta \\ &= \frac{4}{n\pi}\sin\left(\frac{n\pi}{2}\right) \end{aligned} \tag{2.3}$$

$$\begin{aligned} b_n &= \frac{1}{\pi}\int_{-\pi/2}^{3\pi/2} \mathrm{sq}(\theta)\sin(n\theta)\,d\theta \\ &= \frac{1}{\pi}\int_{-\pi/2}^{\pi/2} \sin(n\theta)\,d\theta - \frac{1}{\pi}\int_{\pi/2}^{3\pi/2} \sin(n\theta)\,d\theta \\ &= \frac{4}{n\pi}\cos\left(\frac{n\pi}{2}\right) \\ &= 0 \end{aligned} \tag{2.4}$$

Since sq(ωt) function is an even function all of the b_n coefficients should be zero. The Fourier series for the square wave is

$$\mathrm{sq}(\omega t) = \frac{4}{\pi}\sum_{n=1}^{\infty} \frac{\sin(n\pi/2)}{n}\cos(n\omega t). \tag{2.5}$$

The fundamental component a_1 has an amplitude of 4/π and an RMS value of $2\sqrt{2}/\pi$. Solving for the THD yields the following result.

$$THD_v = \sqrt{\frac{1-\left(\frac{2\sqrt{2}}{\pi}\right)^2}{\left(\frac{2\sqrt{2}}{\pi}\right)^2}} = 48.3\% \qquad (2.6)$$

The graph of the sq(ωt) and the spectrum of the Fourier series expansion are shown in Figure 1.

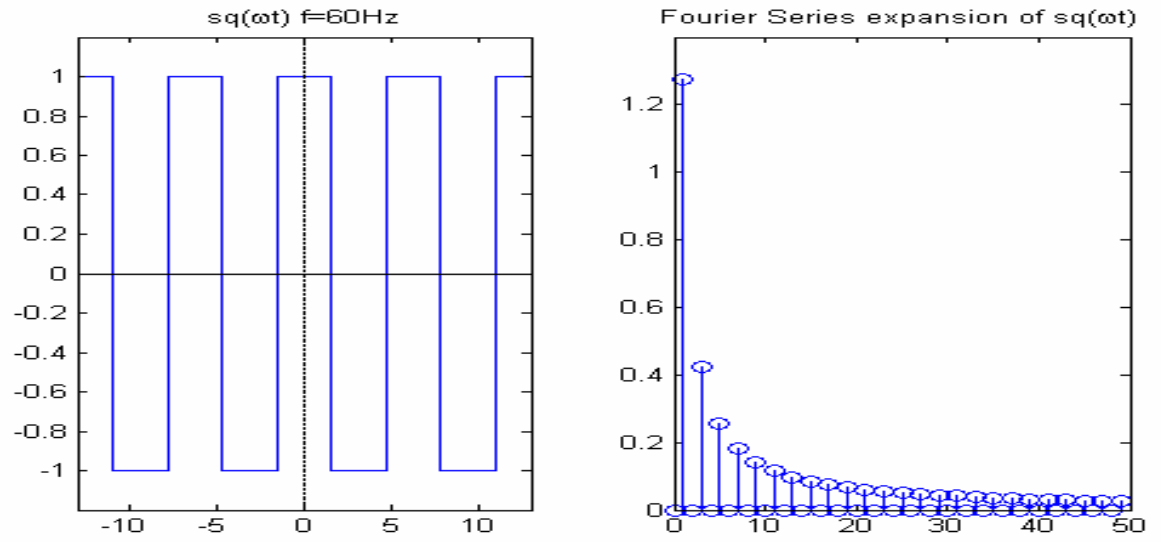

Figure 1 Square Wave and Fourier Series Expansion

C. HALF-BRIDGE INVERTER

One of the simplest ways to realize a square wave as shown in Figure 1 is through the use of a half-bridge inverter as shown in Figure 2.

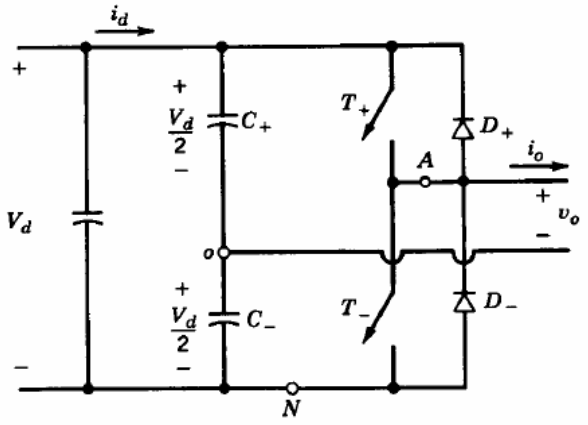

Figure 2 Half-Bridge Inverter
[From Ref 8]

The half-bridge consists of two controllable switches that transform the DC source into a quasi-AC output by switching action. Across each half-bridge switch is a diode, placed in the reverse direction of the switch, to provide a path for inductive loads during switching transition. Two equal valued capacitors are connected in series across the DC voltage source and provide a mid-potential point given symmetrical switching. The capacitors are sufficiently large to keep the midpoint essentially constant with respect to $+V_{DC}$ and $-V_{DC}$. The upper and lower switches should not be closed at the same time since this would create a short-circuit and be potentially damaging to the switches.

The fully controllable switches in the inverter should ideally display the following characteristics:

- The switches should block high forward and reverse voltages with zero current leakage when ‘off’.
- The switches should conduct large current with zero voltage drop when ‘on’.
- The switches should switch from the on-state to the off-state as well as the off-state to the on-state instantaneously when gated.
- The switches should require no power to switch between states or lock the switch in a state either ‘on’ or ‘off’.

However, real world devices do not have these ideal traits. Several types of semiconductor power devices can be used as non-ideal alternatives. These power devices are turned 'on' and 'off' by control signals applied to the gate terminal of the device. Semiconductor power devices will dissipate power when switching. There is a small time period when the switch is transitioning from the on-state to the off-state where both a voltage drop and a current flow exist. Figure 3 illustrates the scenario when a switching transient experiences near maximum values for both current and voltage. As the switching frequency increases and more transition states occur over a set time period, there is a corresponding linear increase in the switching power losses [9].

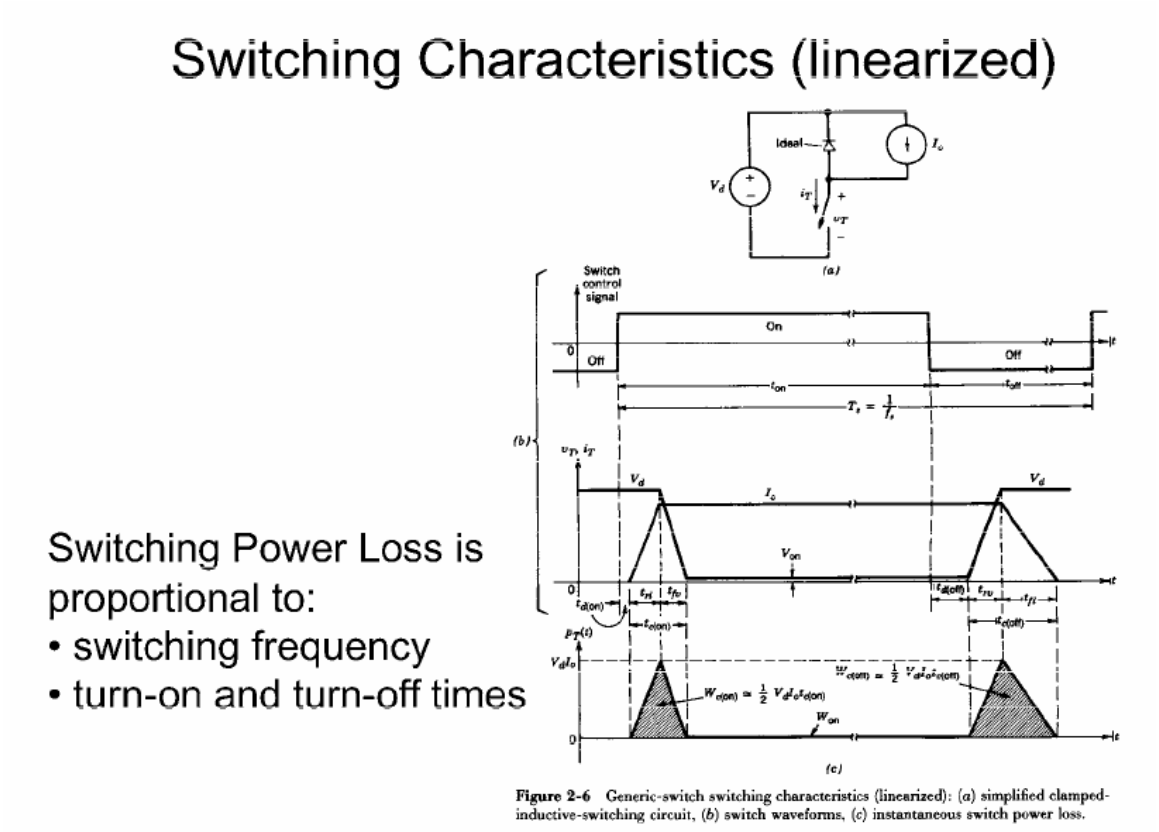

Figure 2-6 Generic-switch switching characteristics (linearized): (*a*) simplified clamped-inductive-switching circuit, (*b*) switch waveforms, (*c*) instantaneous switch power loss.

Figure 3 Power Loss Across a Switch

[From Ref 8]

The choice of which semiconductor device to use as a switch is driven by the power and the switching speed requirements. For this project the IGBT was chosen because of its availability in COTS systems. The IGBT has become dominant in the

power conversion industry and provides the best compromise between available output power and switching frequency for low to medium voltage systems.

D. SIX-STEP THREE-PHASE INVERTERS

Three H-bridges are placed in parallel to create a three-phase output. The six-step switching scheme is sometimes called the 180° voltage source operation or square-wave switching. In this scheme each switch in the inverter is 'on' for one-half cycle (180°) of the desired output frequency. The switches (Figure 4) follow a three-phase cyclic pattern as shown in Table 1. There is a switching event every 60° for the six-step controller strategy as illustrated in Figure 5 [6].

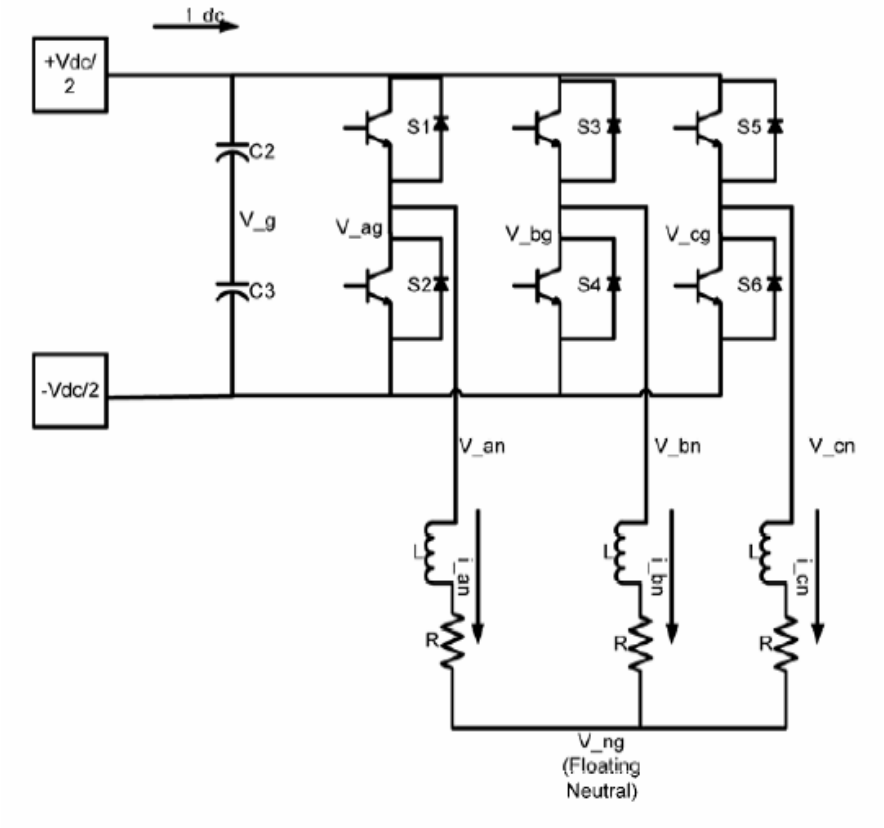

Figure 4 Three Phase Bridge Inverter
[After Ref 9]

Wave portion	Interval *	Switches Closed	Gate Signals
Positive Half	0 to π/3	T1 closed at 0	S1-S4-S5
Negative Half	π/3 to 2π/3	T6 closed π radians after T5	S1-S4-S6
Positive Half	2π/3 to π	T3 closed 2π/3 radians after T1	S1-S3-S6
Negative Half	π to 4π/3	T2 closed π radians after T1	S2-S3-S6
Positive Half	4π/3 to 5π/3	T5 closed 2π/3 radians after T3	S2-S3-S5
Negative Half	5π/3 to 2π	T4 closed π radians after T3	S2-S4-S5
* Set up for a period of 2π, for frequency *f*, divide each term in the interval by *f*			

Table 1 Six-Step Invert Three-phase Cyclic Switching Pattern

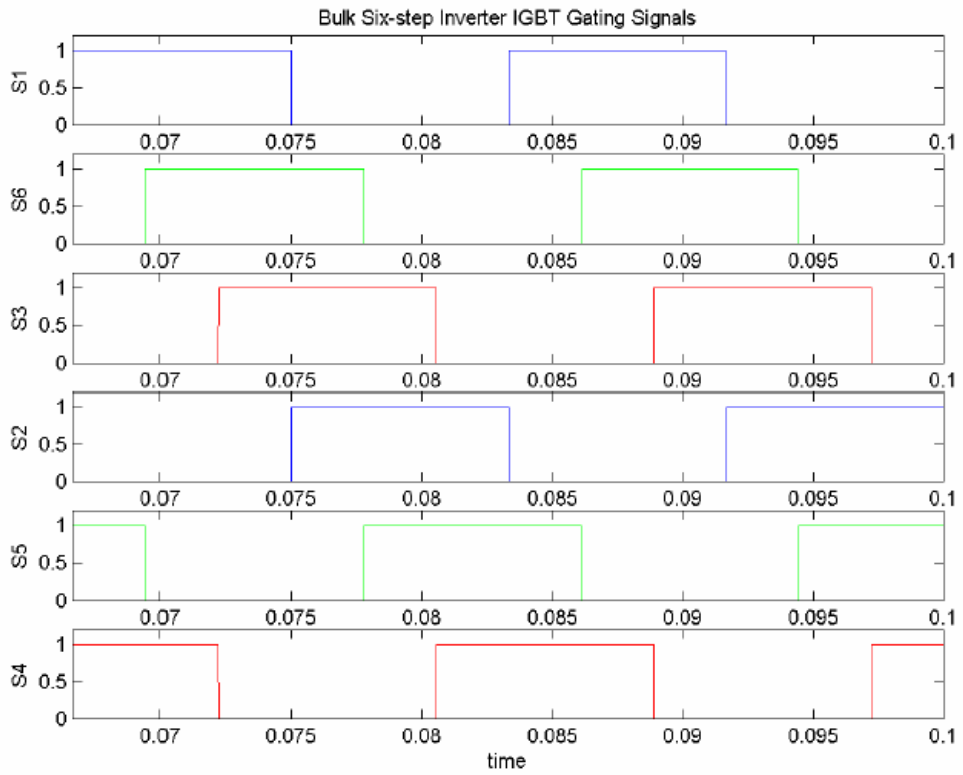

Figure 5 Six-Step Invert Gate Control Signals (f_c=60 Hz)

[After Ref 6]

Table 2 shows the resultant line-to-neutral and line-to-line voltages for each phase. The six step line-to-line voltages are graphed for a frequency of 60Hz as shown in Figure 6 while the line-to-neutral voltages are provided in Figure 7.

V_{DC}=100V	INTERVAL*					
VOLTAGE	0 to π/3	π/3 - 2π/3	2π/3 - π	π - 4π/3	4π/3 - 5π/3	5π/3 - 2π
V_{an}	$\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$-\frac{2}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$
V_{bn}	$-\frac{2}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$
V_{cn}	$\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$-\frac{2}{3}V_{DC}$	$-\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}$	$\frac{2}{3}V_{DC}$
V_{ab}	V_{DC}	V_{DC}	0	$-V_{DC}$	$-V_{DC}$	0
V_{bc}	$-V_{DC}$	0	V_{DC}	V_{DC}	0	$-V_{DC}$
V_{ca}	0	$-V_{DC}$	$-V_{DC}$	0	V_{DC}	V_{DC}
* Set up for a period of 2π, for frequency *f*, divide each term in the interval by *f*						

Table 2 Line-to-Neutral and Line-to-Line Voltages

[After Ref 6]

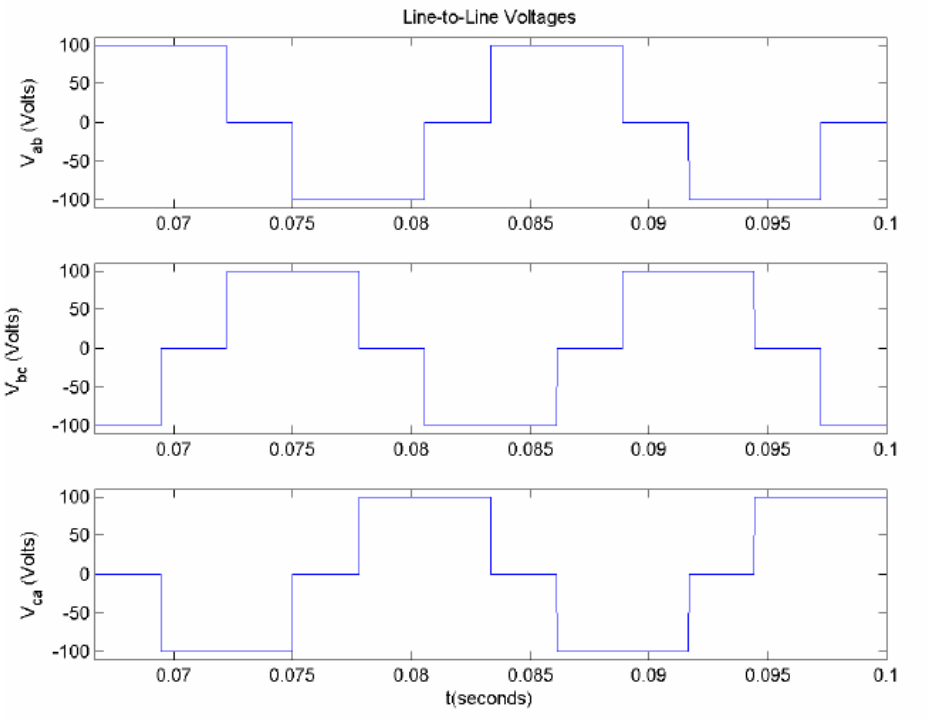

Figure 6 Six-Step Inverter Line-to-Line Voltages 60Hz

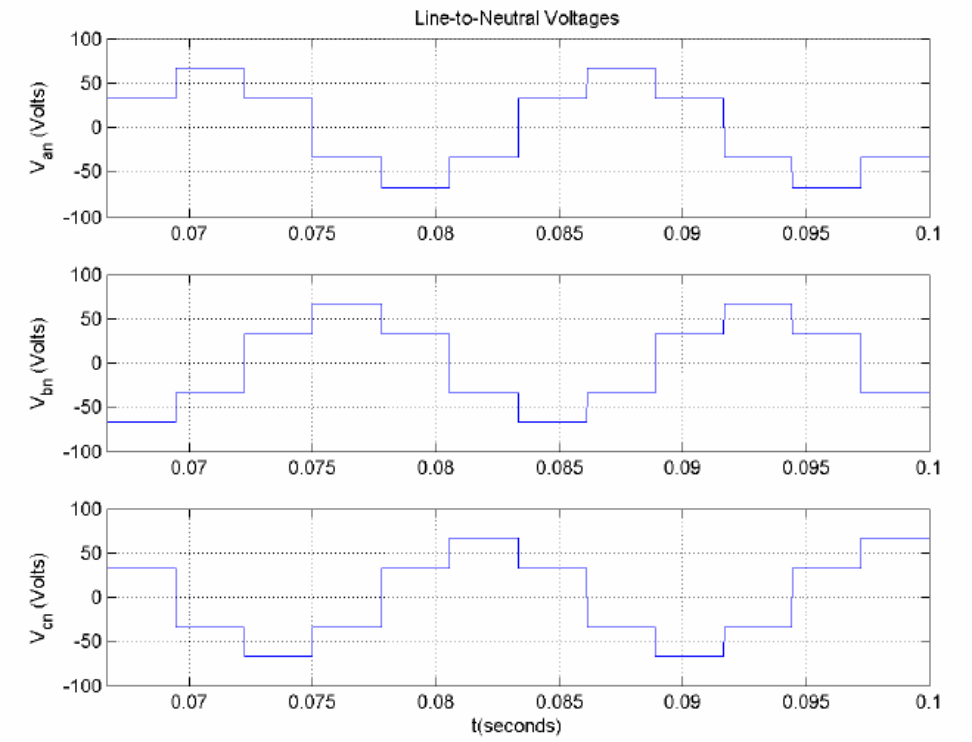

Figure 7 Six-Step Inverter Line-to-Neutral Voltages 60Hz

The line-to-neutral voltage V_{an} as shown in Table 2 can be written as a function of θ.

$$V_{an}(\theta) = \begin{cases} +\frac{2}{3} & \frac{\pi}{3} \le \theta < \frac{2\pi}{3} \\ +\frac{1}{3} & 0 \le \theta < \frac{\pi}{3}, \frac{2\pi}{3} \le \theta < \pi \\ -\frac{1}{3} & \pi \le \theta < \frac{4\pi}{3}, \frac{5\pi}{3} \le \theta < 2\pi \\ -\frac{2}{3} & \frac{4\pi}{3} \le \theta < \frac{5\pi}{3} \end{cases} \tag{2.7}$$

$V_{an}(\theta)$ has an RMS value of $\sqrt{2}/3$. Since $V_{an}(\theta)$ is an odd function the Fourier series coefficients for all of the a_n terms are equal to zero. The b_n terms are computed as shown.

$$
\begin{aligned}
b_n &= \frac{1}{\pi}\int_0^{2\pi} \mathrm{V}_{\mathrm{an}}(\theta)\sin(n\theta)\,d\theta \\
b_n &= \frac{1}{3\pi}\int_0^{\pi/3}\sin(n\theta)\,d\theta + \frac{2}{3\pi}\int_{\pi/3}^{2\pi/3}\sin(n\theta)\,d\theta + \frac{1}{3\pi}\int_{2\pi/3}^{\pi}\sin(n\theta)\,d\theta \\
&\quad -\frac{1}{3\pi}\int_{\pi}^{4\pi/3}\sin(n\theta)\,d\theta - \frac{2}{3\pi}\int_{4\pi/3}^{5\pi/3}\sin(n\theta)\,d\theta - \frac{1}{3\pi}\int_{5\pi/3}^{2\pi}\sin(n\theta)\,d\theta \\
b_n &= \frac{1}{n3\pi}\left[2\cos(n\pi) - \cos\left(\frac{n\pi}{3}\right) + \cos\left(\frac{n2\pi}{3}\right) + \cos\left(\frac{n4\pi}{3}\right) - \cos\left(\frac{n5\pi}{3}\right) - 2\right]
\end{aligned}
\tag{2.8}
$$

The Fourier series for the $\mathrm{V}_{\mathrm{an}}(\theta)$ wave is

$$
\mathrm{V}_{\mathrm{an}}(\theta) = \sum_{n=1}^{\infty} \frac{\left[2\cos(n\pi) - \cos\left(\frac{n\pi}{3}\right) + \cos\left(\frac{n2\pi}{3}\right) + \cos\left(\frac{n4\pi}{3}\right) - \cos\left(\frac{n5\pi}{3}\right) - 2\right]}{3\pi n}\cos(n\theta) \tag{2.9}
$$

The fundamental component b_1 has amplitude of $2/\pi$ and a RMS value of $\sqrt{2}/\pi$. The THD computed as follows.

$$
\mathrm{THD}_{\mathrm{v}} = \sqrt{\frac{\left(\frac{\sqrt{2}}{3}\right)^2 - \left(\frac{\sqrt{2}}{\pi}\right)^2}{\left(\frac{\sqrt{2}}{\pi}\right)^2}} = 31.1\% \tag{2.10}
$$

The graph of $\mathrm{V}_{\mathrm{an}}(\theta)$ and the Fourier series expansion of the spectrum are shown in Figure 8. The spectrum shows that there are no even harmonics and that the odd multiples of three have been eliminated.

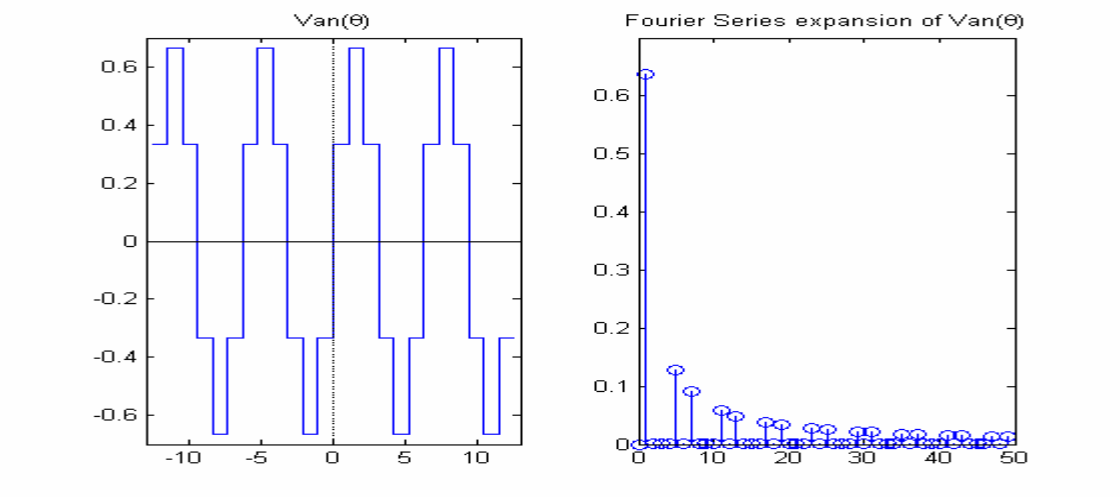

Figure 8 Six-Step Line-to-Neutral Voltage and Harmonics

It is also important to analyze the current wave forms. The complex impedance Z must be used to determine the line-to-neutral current wave forms. The phase-A current is expressed as:

$$I_{an} = \frac{V_{an}}{|Z|} \tag{2.11}$$

where the magnitude of Z is defined by $|Z| = \sqrt{R+j\omega L}$. Because of the inductance in Z, the line-to-neutral current wave will no longer be square as it would with a purely resistive load. The line-to-neutral current wave with R= 10Ω and L=22.5mH at 60Hz for a single phase is shown in Figure 9. A numerical analysis of the six-step three-phase line-to-neutral THD_i ranges from 31.1% for a purely resistive load to 5.6% for a very large inductive load.

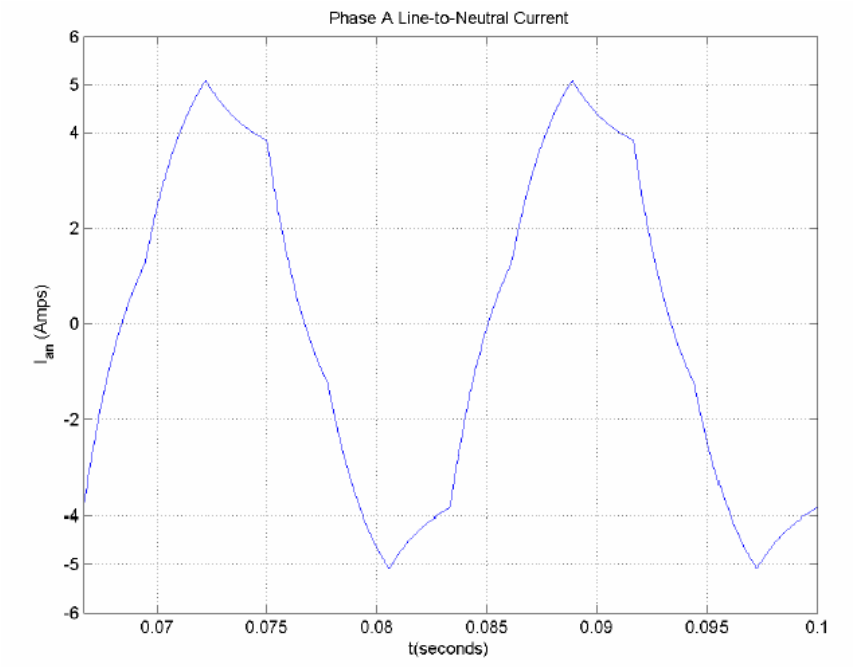

Figure 9 Phase A Line-to-Neutral Current

The principal advantage of using the six-step control method is a minimum number of switching states conducive to minimizing losses for very high power converters. Another advantage is the simplicity of the control strategy. The frequency of the output can be varied by changing the controller frequency. The amplitude of the fundamental generated with the six-step inverter is nearly the largest value that can be obtained using any three-phase topology due to the high third-harmonic content. Unfortunately, there is the penalty of many other undesired harmonics that must be filtered.

There are three principle disadvantages of the six-step control method. First is the considerable harmonic content in the output. Second is that the amplitude of the output can only be controlled by adjusting the amplitude of the DC source. Third is the potential for zero-sequence current. Zero-sequence current is the result of not having a perfectly balanced system. If not controlled, the zero-sequence current will result in significant power losses and instability.

E. HYSTERESIS CONTROLLED CURRENT-SOURCE INVERTER

Passive filters can be constructed to filter out unwanted harmonic content and reduce the THD. In order to construct a passive filter capable of meeting the Navy standards, it would need to be very large and heavy. An alternative is an active filter that requires a power source to actively remove unwanted harmonic content. A second six-step inverter placed in parallel with the bulk inverter can act as an active filter. The control method chosen to run the active filter for this thesis is a hysteresis control algorithm.

The hysteresis control consists of a reference sine wave I_{ref} and a predetermined allowed variation, $2\Delta h$. The allowed variation is translated into an upper limit by adding Δh and lower limit by subtracting Δh from I_{ref} as shown in Figure 10.

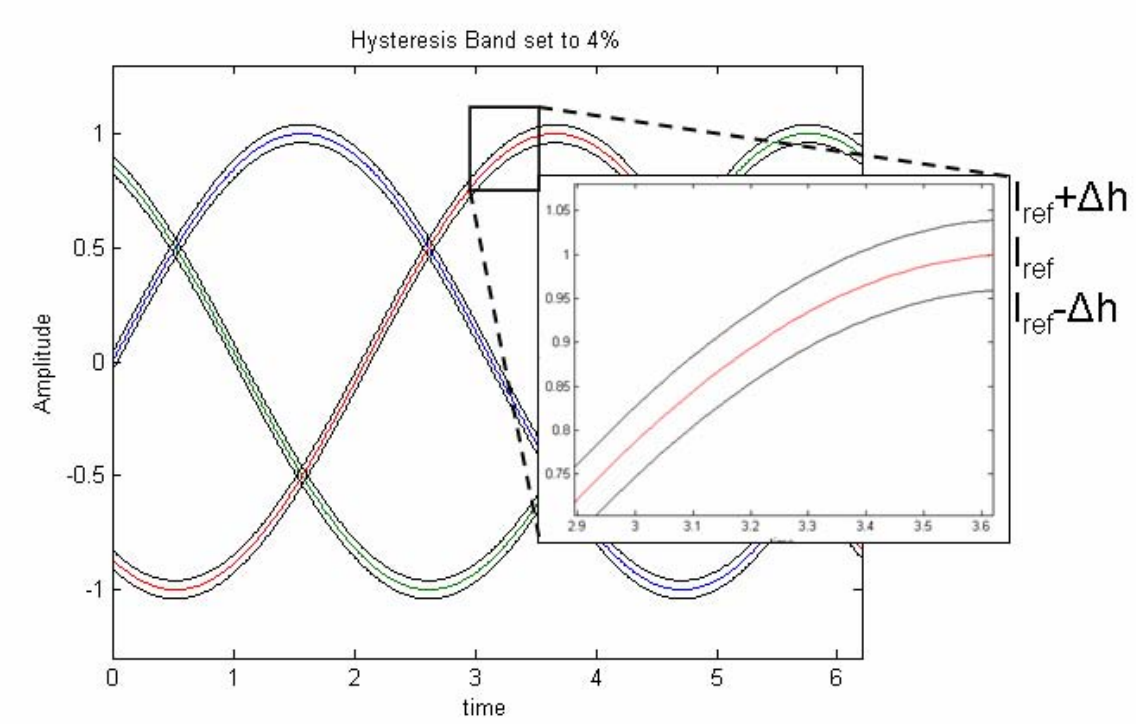

Figure 10 Hysteresis Bands(4% ripple)

The hysteresis controller will keep the load current inside this band by comparing the output signal I_o to the reference signal. When I_o exceeds the upper bound ($I_{ref} + \Delta h$) the controller changes states to apply negative voltage, $-V_{DC}$. This drives I_o back into the acceptable band. When I_o exceeds the lower bound ($I_{ref} - \Delta h$) the controller changes

states to apply positive voltage, $+V_{DC}$. This drives I_o back up into the acceptable band. When I_o is within the band the switch states remain unchanged. In control theory this is sometimes called a 'bang-bang' controller because it bounces from limit to limit. Table 3 demonstrates the logic behind the hysteresis controller for each of the three phases and switching states of the switches. Figure 11 shows an example of a single-phase hysteresis controlled sine wave.

LOGIC	SWITCH	SWITCH POSITIONS
$i_{oa} \leq i_{refa} - \Delta_h$	Set $V_{ag} = \frac{V_{dc}}{2}$	T1 is ON and T2 is OFF
$i_{refa} - \Delta_h \leq i_{oa} \leq i_{refa} + \Delta_h$	No Change	Unchanged
$i_{oa} \geq i_{refa} + \Delta_h$	Set $V_{ag} = \frac{-V_{dc}}{2}$	T2 is ON and T1 is OFF
$i_{ob} \leq i_{refb} - \Delta_h$	Set $V_{bg} = \frac{V_{dc}}{2}$	T3 is ON and T4 is OFF
$i_{refb} - \Delta_h \leq i_{ob} \leq i_{refb} + \Delta_h$	No Change	Unchanged
$i_{ob} \geq i_{refb} + \Delta_h$	Set $V_{bg} = \frac{-V_{dc}}{2}$	T4 is ON and T3 is OFF
$i_{oc} \leq i_{refc} - \Delta_h$	Set $V_{cg} = \frac{V_{dc}}{2}$	T5 is ON and T6 is OFF
$i_{refc} - \Delta_h \leq i_{oc} \leq i_{refc} + \Delta_h$	No Change	Unchanged
$i_{oc} \geq i_{refc} + \Delta_h$	Set $V_{cg} = \frac{-V_{dc}}{2}$	T6 is ON an d T7 is OFF

Table 3 Hysteresis Controller Logic

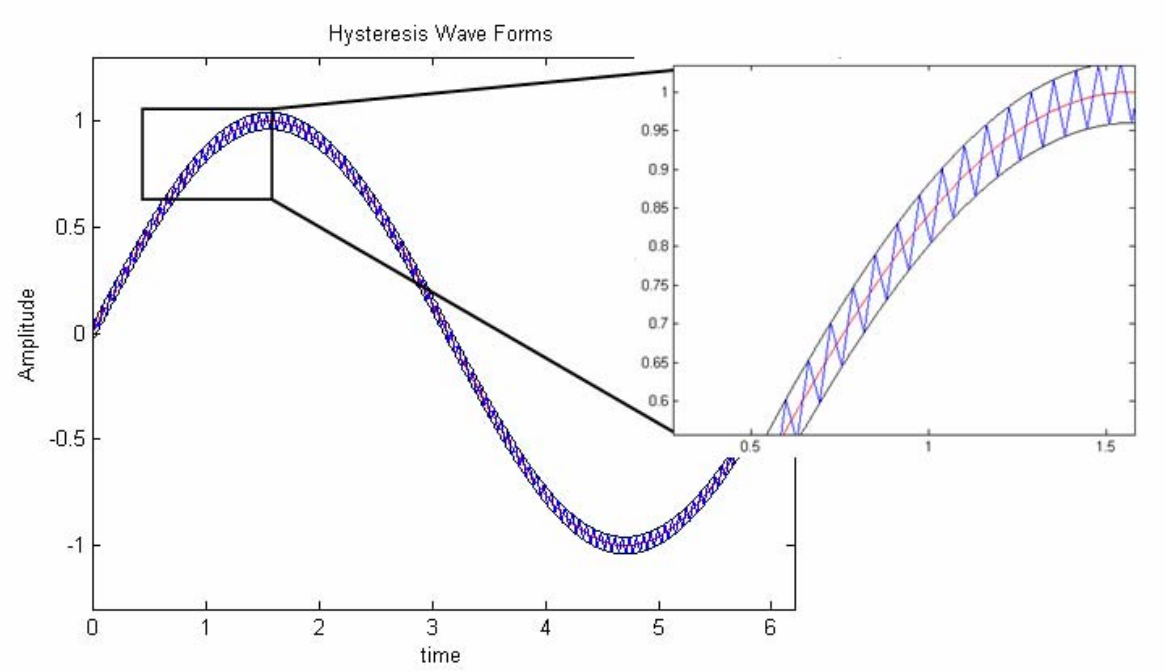

Figure 11 Hysteresis Single-Phase Switching

The size of Δh sets an upper limit on amount of THD. Reducing Δh to zero would reduce the THD_i to zero. Unfortunately, this would require an infinite switching speed impossible in the real world. The result of excessive switching frequency is 'chatter'; 'chatter' is a state similar to aliasing where states become defined by circuit characteristics other then control bandwidth. This can cause several problems with solid-state devices including circuit malfunction and switch destruction. The PEBB used in this thesis has a switching frequency limit of 20kHz.

Two previous theses at NPS implemented parallel hysteresis control algorithms with some success. The first by Terrance White resulted in a THD_i of 3.2% [10]. The second by Bradford Bittle achieved a THD_i of 1.8% [6].

F. POWER ELECTRONIC BUILDING BLOCKS

PEBBs are power processors. A PEBB is not a specific semiconductor material, device, or circuit topology. It is the search for the common electrical, mechanical and thermal denominators of all converter topologies to allow the integration of multiple technologies [11]. This means that one common 'brick' can be used in many power

electronic converters. The PEBB becomes a “plug and play” solution for power conversion. The PEBB program, conceived by Office of Naval Research (ONR), was initiated in late 1994 [12]. Currently several companies are working on producing PEBBs. The PEBB chosen for this project was produced by SEMIKRON as an educational demonstrator. The basic schematic for the SEMIKRON PEBB is shown in Figure 12. The specifications are included in Appendix C.

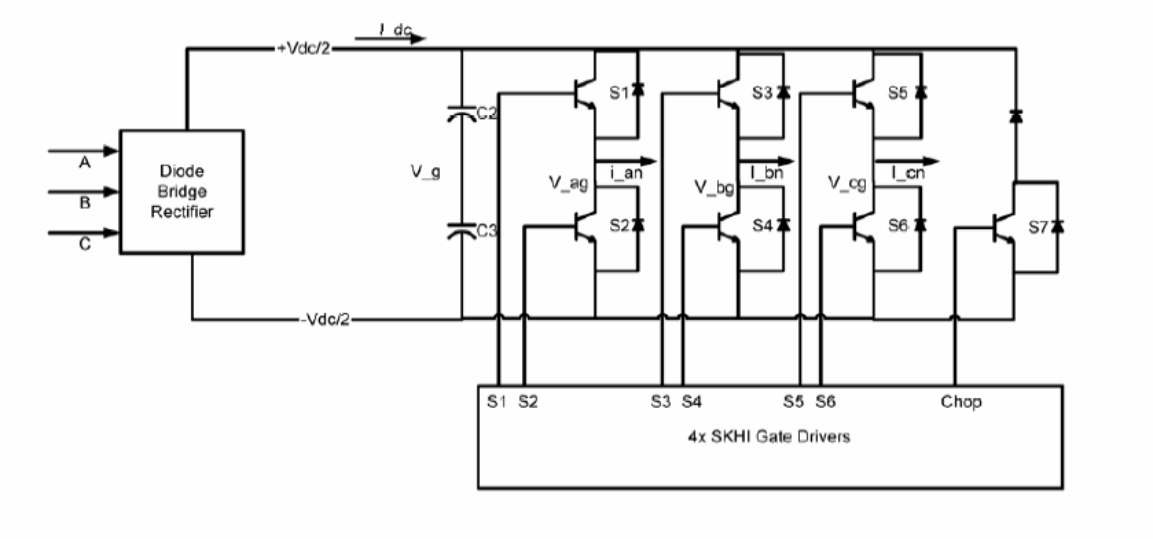

Figure 12 SEMIKRON PEBB

[After Ref 13]

G. FIELD PROGRAMMABLE GATE ARRAYS

An FPGA is a generic semiconductor device containing a large number of programmable logic components and interconnects. The logic components can be programmed to duplicate the functionality of basic gates such as AND, OR, XOR, and NOT, and simple math functions. The hierarchy of the programmable interconnects allows the logic blocks of an FPGA to be interconnected as needed by the system designer. These logic interconnects can be ‘programmed’ after the manufacturing process by the user in the ‘field’. The above promptly uncovers the origin of the name.

The historical roots of the FPGA are in the Complex Programmable Logic Devices (CPLD) of the early 1980s. The CPLD contained several thousand logic gates, while the FPGA can contain over a million. The first FPGA was introduced in 1985 by XILINX® corporation [14]. The primary difference between the CPLD and the FPGA is

architecture. A CPLD is a restrictive structure consisting of one or more programmable sum-of-products logic arrays feeding a clock registrar. The FPGA is dominated by interconnects and high level embedded functions [15].

Today there are several different companies that manufacture FPGAs and there are an ever increasing number of high level tools that make the programming of the FPGA fast and easy. One such tool is the SIMULINK® inside of MATLAB® given appropriate added libraries from the chip manufacturer. The increased processing power of the FPGA means that the controls of the PEBB previously done by several different cards can now be consolidated into a single controller. For this project, a XILINX® Virtex-II™ chip was chosen. The specifications are included in Appendix C.

H. SUMMARY

This chapter provided an overview of the major concepts that will be explored in this research effort. The next chapter will expound on the computer modeling and simulation.

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III. COMPUTER MODEL AND SIMULATIONS

A. OVERVIEW

This chapter describes the computer modeling and the simulation results. The major components are modeled mathematically using SIMULINK®. The FPGA performance is also modeled in SIMULINK® using the XILINX® block set. The XILINX® block set must be purchased as add-on software to SIMULINK®. When complete the model predicts how all aspects of the system work.

Certain assumptions are made to simplify the model. First, the load is assumed to be a balanced three-phase linear impedance. Second, the model is temperature independent which means there is no time-variance in the output due to system heating or cooling. Third, the IGBTs are ideal switches with no switching delays, no current leakage and no voltage drops. There are no resistive losses other than those associated with the load. Even with these assumptions, the model is quite accurate.

Figure 13 is a diagram of the overall system model. There are three main sections. First (from right to left), the *Load* section outlined in "– – –" (green) represents the load on the system. Second, the *PEBB* section outlined in "·· –" (gold) represents the PEBB purchased from SEMIKRON. Third, the *Control* section outlined in "–" (blue) represents the functions completed by the FPGA and NPS custom built controller card. Each of the sections will be discussed in more detail.

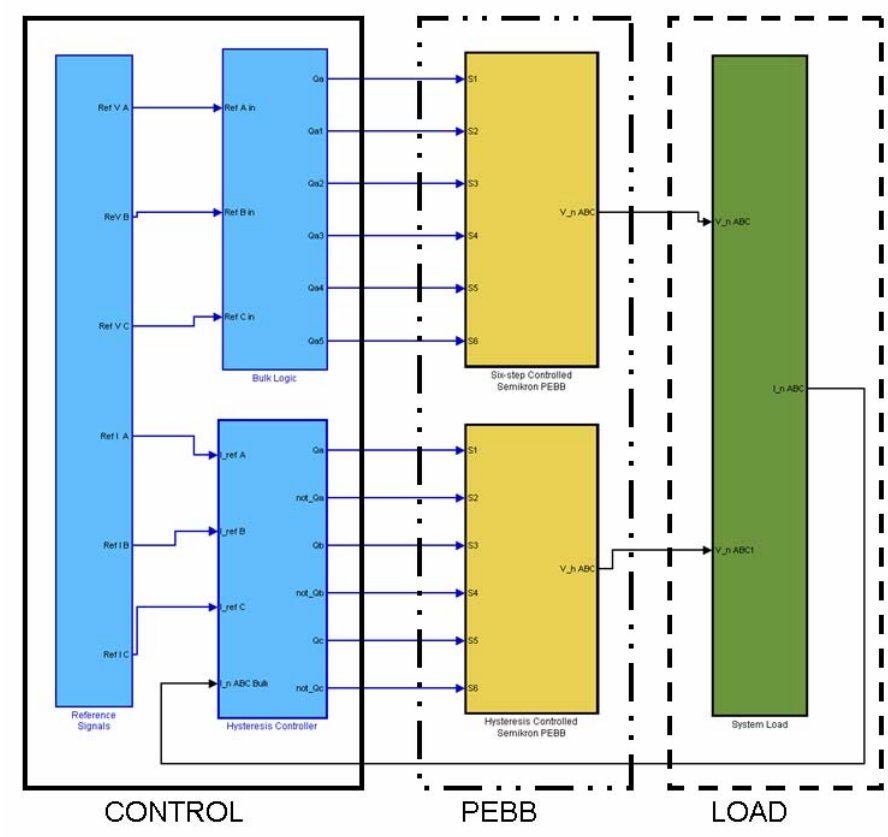

Figure 13 System Model

B. LOAD MODEL

The load in Figure 13 consists of both resistive and inductive elements. A component diagram is shown in Figure 14. Starting from the output of each PEBB there are coupling reactors necessary for limiting the interaction between the PEBBs. The reactors feed current to a delta-connected isolation transformer. The isolation transformer prevents ground loops between PEBB sections and eliminates the need for a zero-sequence loop in the system controller. The isolation transformers are then paralleled into a load representing a motor. The load is a balanced three-phase wye connected series resistance and inductance. Component values are listed in Table 4.

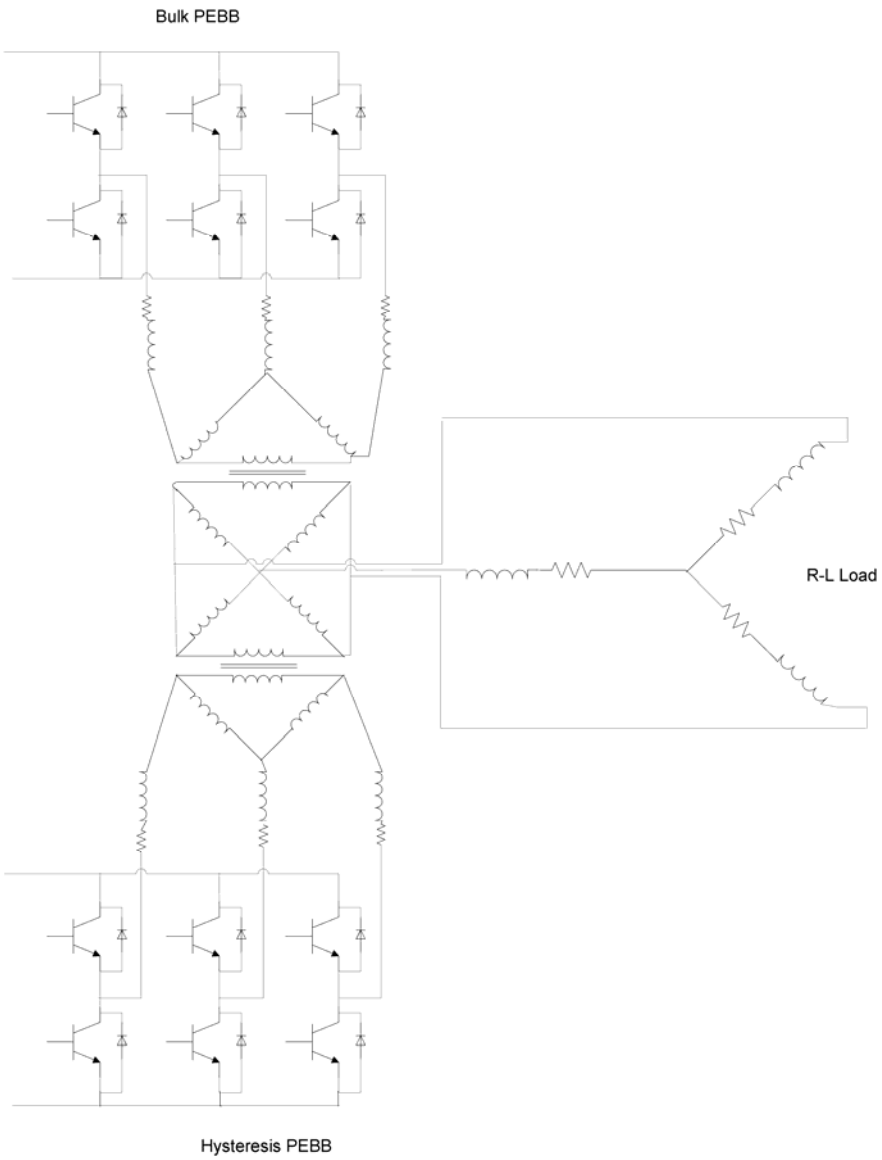

Figure 14 Load Schematic

Symbol	Meaning	Value
R_c	Coupling Resistance	0.025Ω
R_l	Load Resistance	10Ω
L_c	Coupling Inductance	2.5mH
L_l	Load Inductance	20mH

Table 4 Load Symbols and Values

The load is modeled using Kirchhoff's Voltage Law (KVL)

$$I=\frac{V}{Z} \tag{3.1}$$

where

$$Z=\left(L_c+L_l\right)s+\left(R_c+R_l\right). \tag{3.2}$$

The system load model is a series of six transfer functions as seen in Figure 15. The load is the same for both the bulk inverter and the hysteresis inverter, but was easier to simulate via separate channel prior to summing.

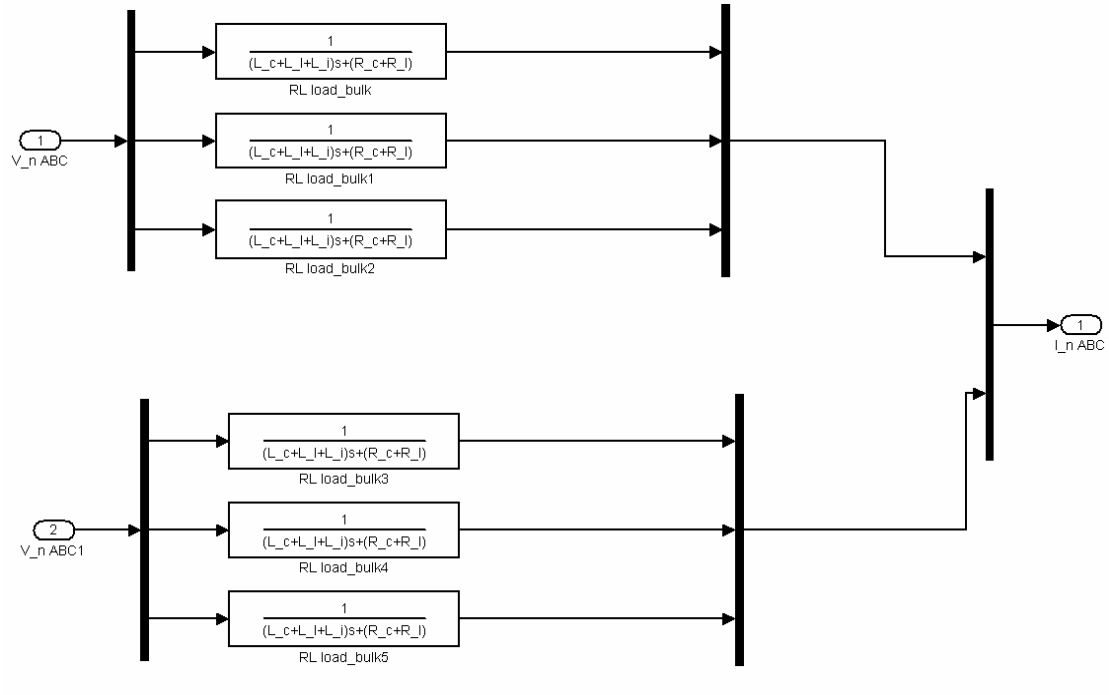

Figure 15 Load Module

C. POWER BLOCK MODELS

Both PEBB modules are identical in operation. The model utilizes six ideal binary position switches to simulate three IGBT half-bridges. The PEBB block for the bulk controller is expanded in Figure 16. The six switch positions are driven by gate signals provided from the FPGA through the NPS custom interface card.

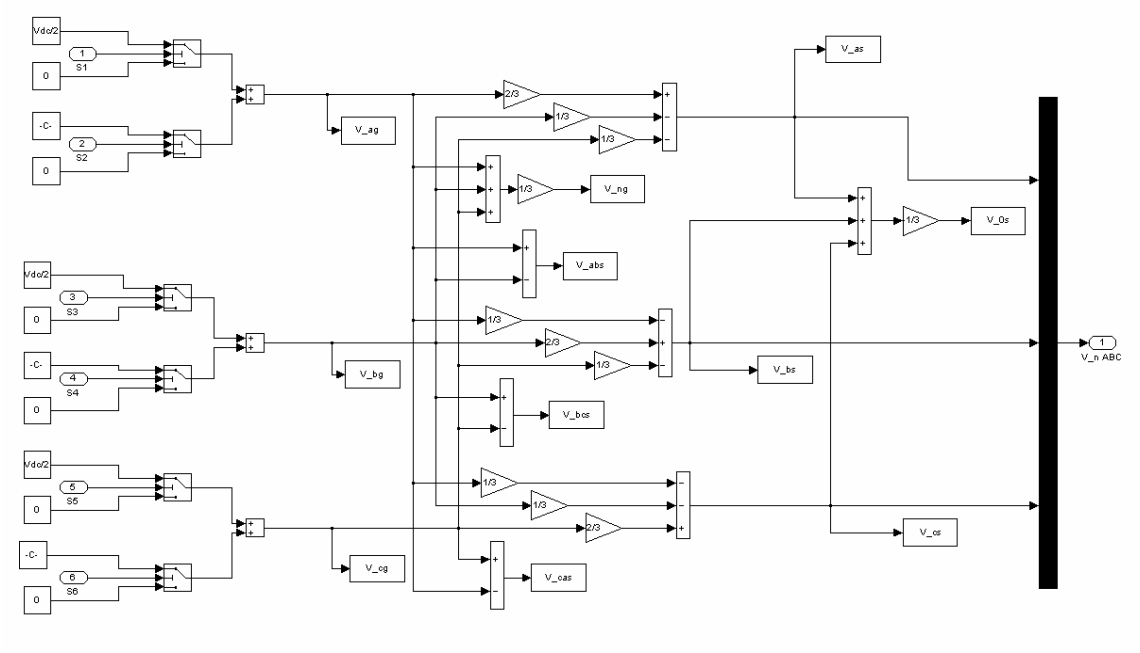

Figure 16 Bulk Six-step Controlled PEBB Module

The single-phase line-to-ground voltages of the three legs are show as v_{ag}, v_{bg}, and v_{cg}. The line-to-neutral voltages are designated v_{an}, v_{bn} and v_{cn}. The line-to-ground voltages are referenced from the midpoint of the IGBT half-bridge for each phase to the mid-potential point between the capacitors. The line-to-neutral voltages are referenced from the midpoint of the IGBT half-bridges to the center of the wye-connected load [6]. The line-to-line voltages can be calculated by:

$$\begin{aligned} v_{ag} &= v_{an} - v_{ng} \\ v_{bg} &= v_{bn} - v_{ng} \\ v_{cg} &= v_{cn} - v_{ng} \end{aligned} \tag{3.3}$$

The system is wye-connected and the relationship between the line-to-neutral and line-to-line voltages is:

$$\begin{aligned} v_{ab} &= v_{ag} - v_{bg} \\ v_{bc} &= v_{bg} - v_{cg} \\ v_{ca} &= v_{cg} - v_{ag} \end{aligned} \tag{3.4}$$

where

$$v_{ng} = \frac{1}{3}\left(v_{ag} + v_{ag} + v_{cg}\right) - \frac{1}{3}\left(v_{an} + v_{bn} + v_{cn}\right) \tag{3.5}$$

Since the loads are identical there is no zero-sequence current loop. This is only true in the ideal model and never in the real world. This is why the isolation transformers were added previously. For the ideal balanced loads

$$v_{an} + v_{an} + v_{cn} = 0. \tag{3.6}$$

Solving equation 0.7 for the line-to-neutral voltages yields the following results:

$$\begin{aligned} v_{an} &= \left[\frac{2}{3} v_{ag} - \frac{1}{3} v_{bg} - \frac{1}{3} v_{cg} \right] \\ v_{bn} &= \left[\frac{2}{3} v_{bg} - \frac{1}{3} v_{ag} - \frac{1}{3} v_{cg} \right] \\ v_{cn} &= \left[\frac{2}{3} v_{cg} - \frac{1}{3} v_{bg} - \frac{1}{3} v_{ag} \right] \end{aligned} \tag{3.7}$$

These calculations form the basis for the PEBB model voltage outputs. The expected wave form can be seen and were given previously in Figure 7.

D. FPGA MODELS

The FPGA portion is broken into three sections that can be seen in Figure 13. They are the *Reference Signals*, *Bulk Logic* and *Hysteresis Controller*. Each section will be discussed in more detail.

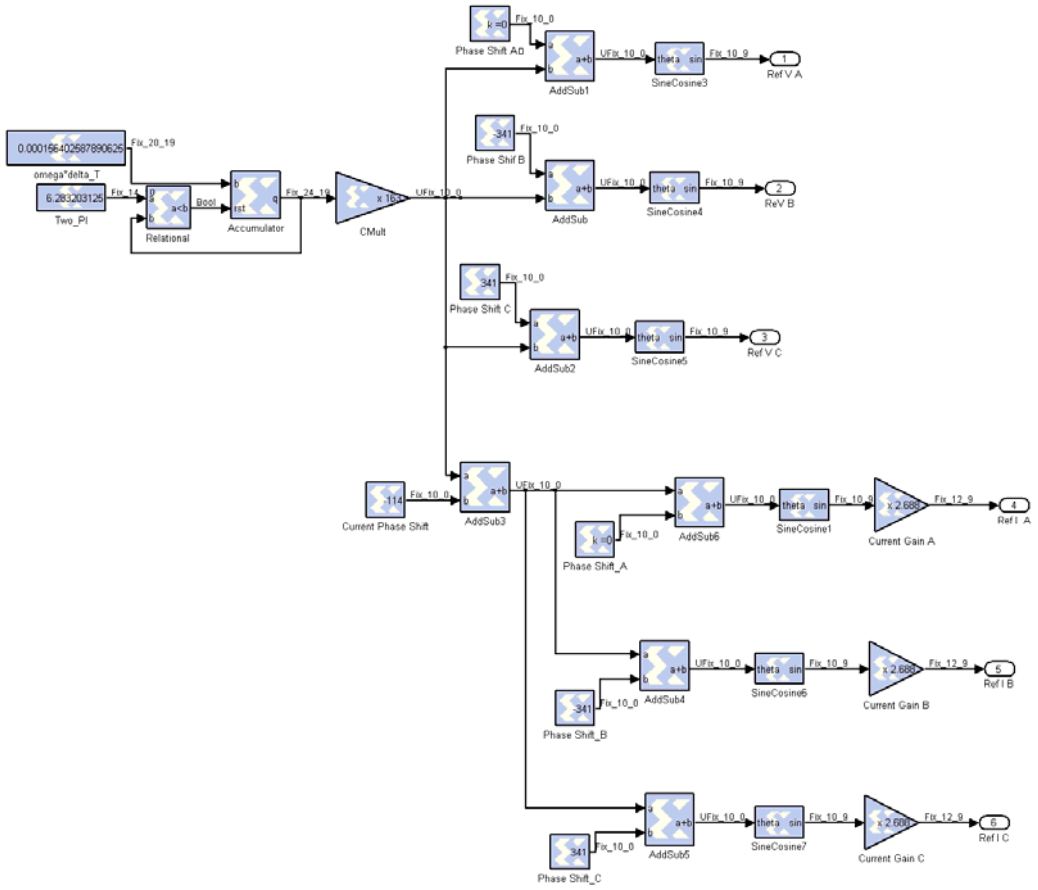

Figure 17 Reference Signals Section

1. Reference Signals Section

The *Reference Signals Section* is show in Figure 17. The purpose of this section is to generate reference voltage and current waves for each of the three phases.

The time to complete one logical operation inside the FPGA is a function of how complex the required sets of operations are. The SIMULINK® model predicts the fastest time to complete one logical step. For the models used in this thesis, the fastest time step achieved was 41.67ns which corresponds to a clock speed of 24MHz. The size of the time step is an important value needed throughout the modeling process and is stored as in the variable *tstep.* A repeating counter is constructed to count from 0 to 2π based on the value of *tstep* and the desired output frequency.

The output signal from the counter is sent to a *SineCosine* function block to produce the phase-A reference voltage wave. Phase-B and phase-C reference voltage waves are produced by adding the appropriate phase shift constant before being sent to *SineCosine* function block. The amplitude of the voltage waves is not used in any modeling so no amplification correction is applied. The three reference voltage waves are processed as 10-digit binary words and then sent to the *Bulk Six-Step Controlled PEBB Logic Module* (Figure 16 Bulk Six-step Controlled PEBB ModuleFigure 16).

The reference current waves must be corrected for phase and amplitude. The phase shift induced by the load is calculated and added to the output of the counter. For phase-B and phase-C a constant representing the appropriate 120° phase shift is also added. The amplitude of the *Current Gain* constant for the reference current wave is calculated taking into account the voltage, impedance and change from delta to wye topology.

$$Current\ Gain = \left| \frac{\frac{2}{3} V_{DC}}{\sqrt{R_{total} + j\omega L_{total}}} \right| \times \sqrt{3} \tag{3.8}$$

2. Bulk Logic Section

The *Bulk Logic Section* as shown in Figure 18 receives the incoming reference waves and performs a polarity check using the *Threshold* function. The output of the *Threshold* function is used to drive the *Bulk Six-Step Controlled PEBB Logic Module*. The blocks labeled *U38-U43* and *U51* are the hardware-in-the-loop interface ports used to acquire the signals that drive the PEBB. This will produce the output predicted in chapter II Figure 5

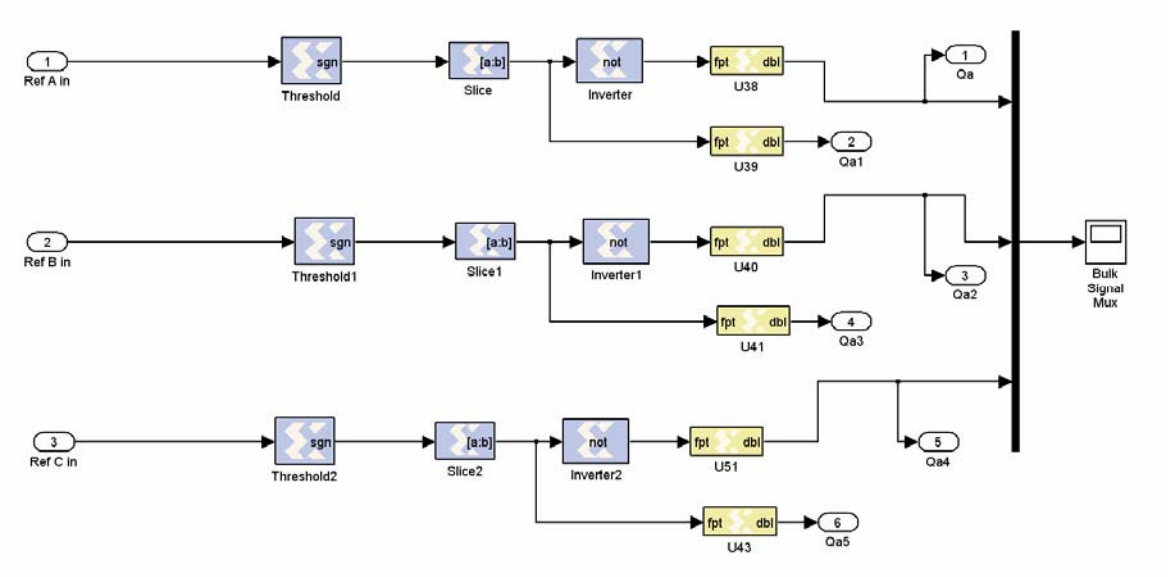

Figure 18 Bulk Logic Section

3. Hysteresis Controller Section

The *Hysteresis Controller Section* shown in Figure 19 has two major sub-sections. The first sub-section models the Analog-to-Digital (A/D) process. The second sub-section provides the hysteresis control logic.

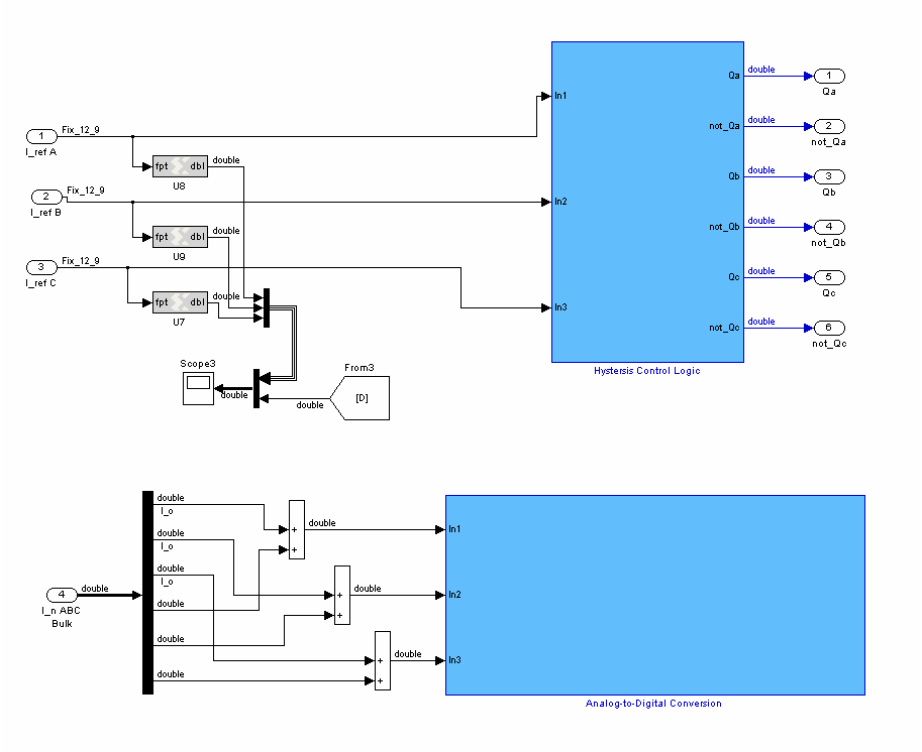

Figure 19 Hysteresis Controller Section

The *Analog-to-Digital Conversion* sub-section shown in Figure 20 receives the combined sampled current signal input from the A/D converter through the *Data_In* block. The combined sampled current signal is separated into the original four digitized sampled current signals. Only three of these signals are used in this application one for each phase. This section of the code contains the timing signals sent out to the A/D converter indicating when to sample. The sample rate is set at 1.5MHz.

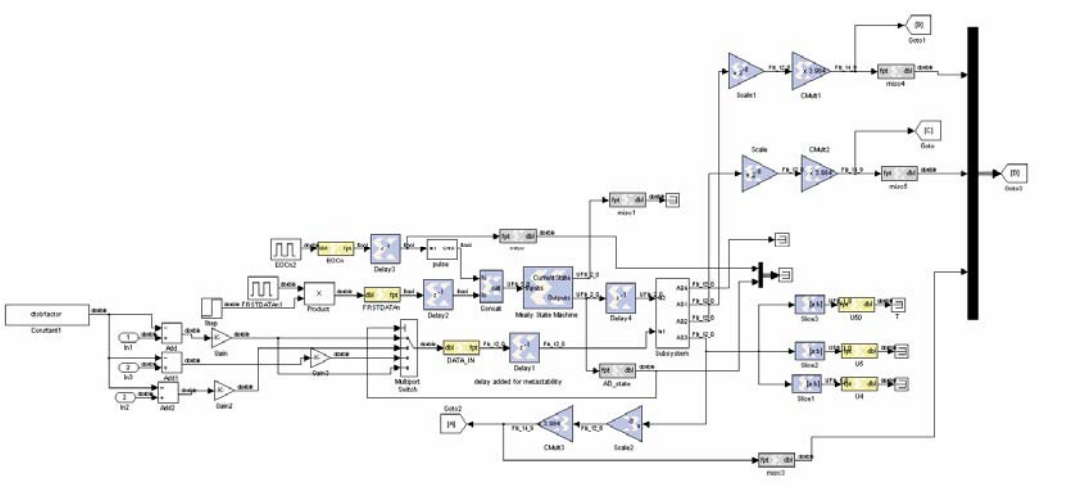

Figure 20 Analog-to-Digital Conversion Sub-Section

The *Hysteresis Control Logic Sub-Section* shown in Figure 21 compares the reference current received from the *Reference Signals Section* (Figure 17) with the measured current received from the *Analog-to-Digital Conversion Sub-Section* (Figure 20). Each of the three phases is handled in exactly the same manner. The software equivalent of an SR flip-flop is used to compare the signals and drive the output of the hysteresis controlled PEBB. In order to not exceed the switching limits of the PEBB a software delay is added to the SR flip-flop function. A counter is incremented at each *tstep* and no change to gating signals is permitted until the counter reaches 1200 which limits switching events to a maximum frequency of 20kHz. If the sampled current is greater then reference current plus the error, and the counter is greater than 1200 then R=1. If the sampled current is less than reference current minus the error, and counter is greater than 1200 then S=1. The truth table for this function is shown as

Table 5. Since the sampled current cannot be both greater than and less than the reference signal at the same time the undefined state is avoided. The output Q is used to drive the hysteresis controlled PEBB. The blocks labeled *U44-U49* are the hardware-in-the-loop interface ports used to acquire the signals that drive the PEBB. The complete model diagrams for the entire system including MATLAB® initialization and function files are included as Appendix A.

Counter	S	R	Q	$\overline{Q}$
<1200	0	0	No Change	No Change
≥1200	0	0	No Change	No Change
<1200	0	1	No Change	No Change
≥1200	0	1	0	1
<1200	1	0	No Change	No Change
≥1200	1	0	1	0
<1200	1	1	Undefined	Undefined
≥1200	1	1	Undefined	Undefined

Table 5 S-R Software Function Truth Table

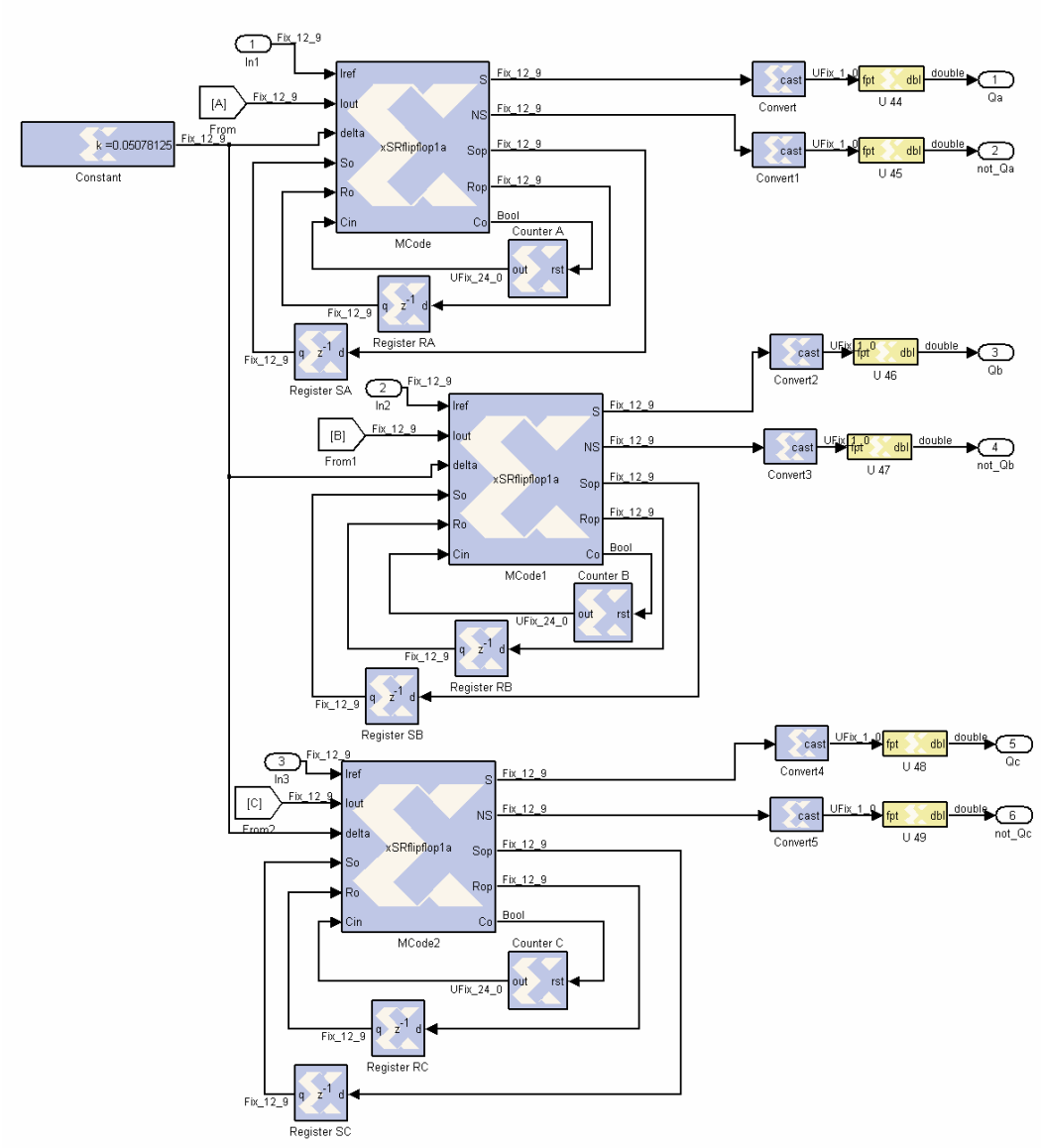

Figure 21 Hysteresis Control Logic Sub-Section

E. RESULTS

One of the advantages to constructing a complete system model in SIMULINK® is that there are many aspects of the model that can be explored, monitored and studied. Important results presented here include the system hardware model, switching performance and the line-to-neutral current characteristics.

1. System Hardware Model

The system hardware model includes all aspects of the hardware. The most complex was the A/D converter interface with the FPGA. Several iterations of the model were required to correctly represent the hardware operation. The largest obstacle was the inclusion of appropriate delays into the model that reflected the actual processes performed inside the A/D converter.

2. Switching Performance

The initial model did not restrict the speed at which gating signals were changed. After running the model and examining the switching speed, some of the gating events were at a frequency of 150kHz. This exceeded the limit of the PEBB. As mentioned, software delays were added to ensure that gating events did not occur at a frequency greater than 20kHz.

3. Line-to-Neutral Current Characteristics

The line-to-neutral current wave forms are of most interest since this project strived to improve their respective THD values. The six-step three-phase line-to-neutral current is shown in Figure 22. The THD for the six-step line-to-neutral phase-A current is calculated in MATLAB® by using a Fourier series expansion as 7.5%. The code for the calculations is included in Appendix A. Because of the symmetrical operation, the theoretical current THD for phases B and C are also 7.5%.

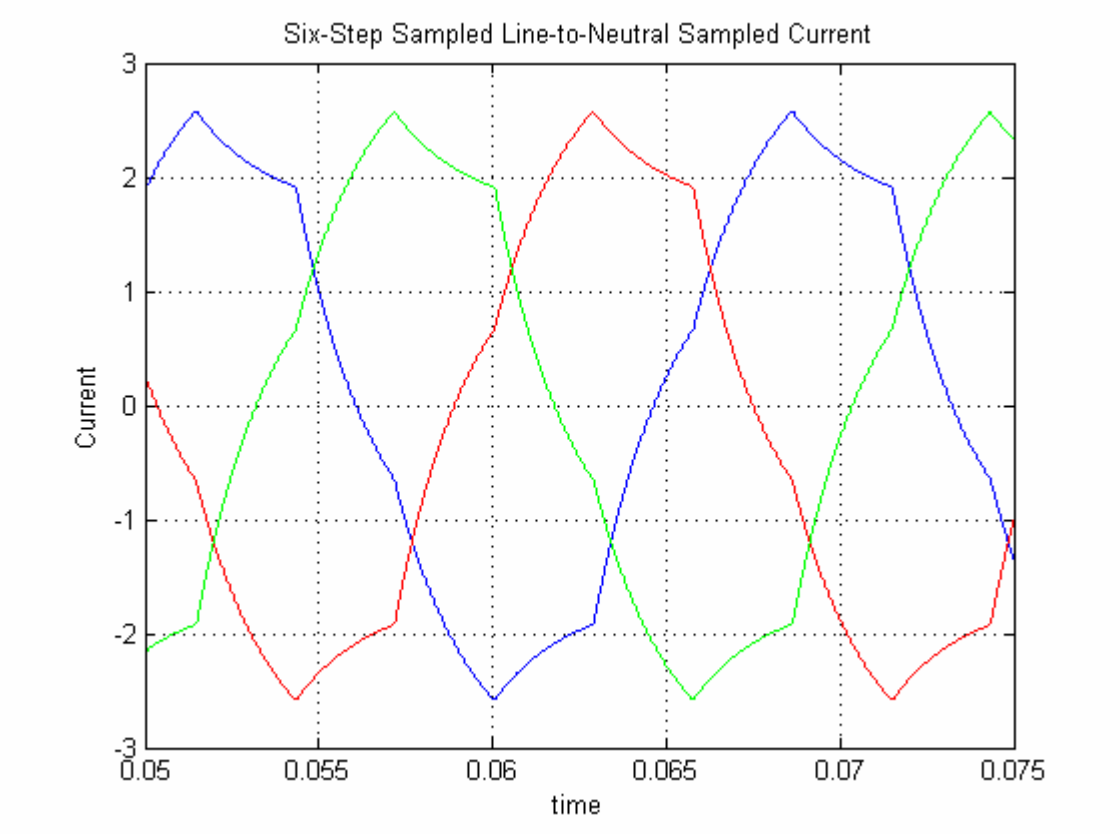

Figure 22 Six-Step Three-Phase Line-to-Neutral Sampled Current

The spectrum showing the first twenty harmonics is depicted in Figure 23. The first twenty harmonics were chosen primarily because of test equipment limitations. This allows for comparison between the models predicted results and the actual results. The noise floor is set to -55dB. The theory suggests that the second, third and fourth harmonics should be at or below the noise floor. This could be due to aliasing from higher frequency components or due to round off errors or noise from the A/D model.

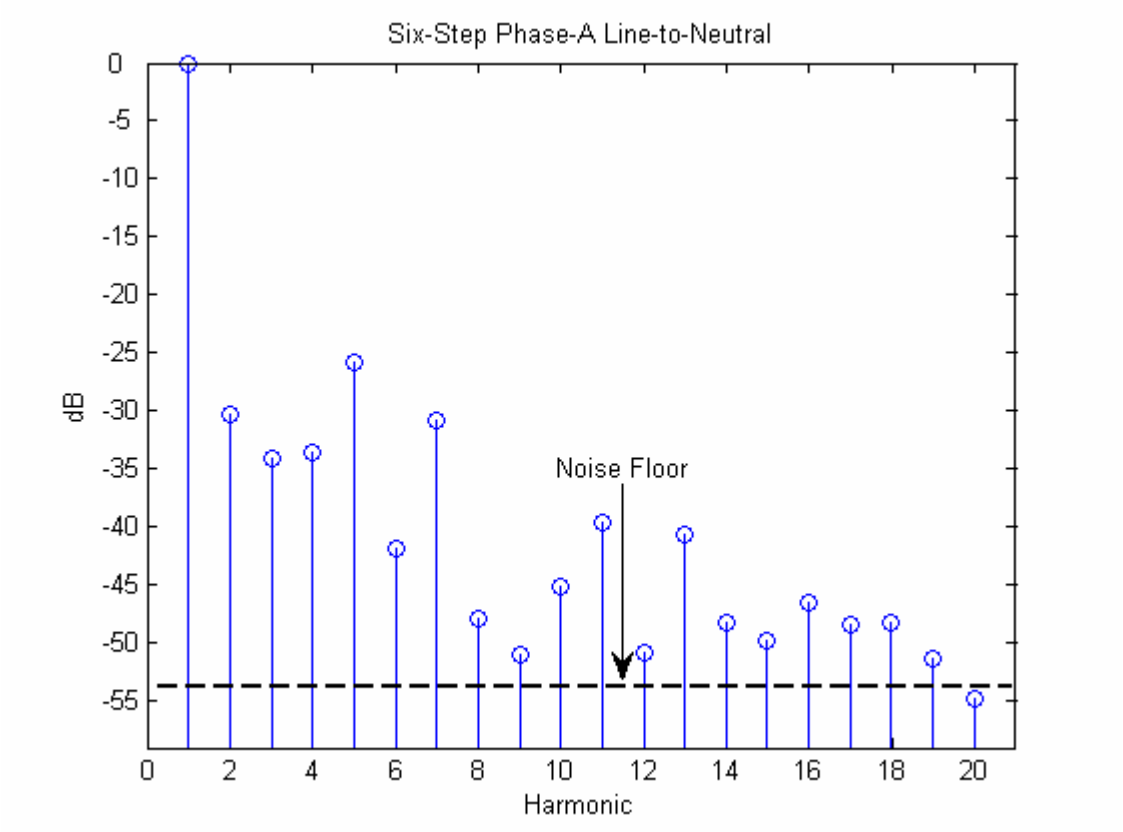

Figure 23 Bulk Current Harmonic Content

With the hysteresis controller activated, the line-to-neutral three-phase current waves are shown in Figure 24. These waves are much more sinusoidal than without the hysteresis filter. However, there is a clear indication of higher frequency harmonics. The *delta_h* parameter sets an upper bound on the value of THD; in this case, *delta_h* was set to 0.05. If there was no limit on switching speed, *delta_h* could continually be reduced until the desired THD was reached. The value for *delta_h* was reached by experimentation. Further work could be done on optimizing this parameter and balancing it with the switching speeds.

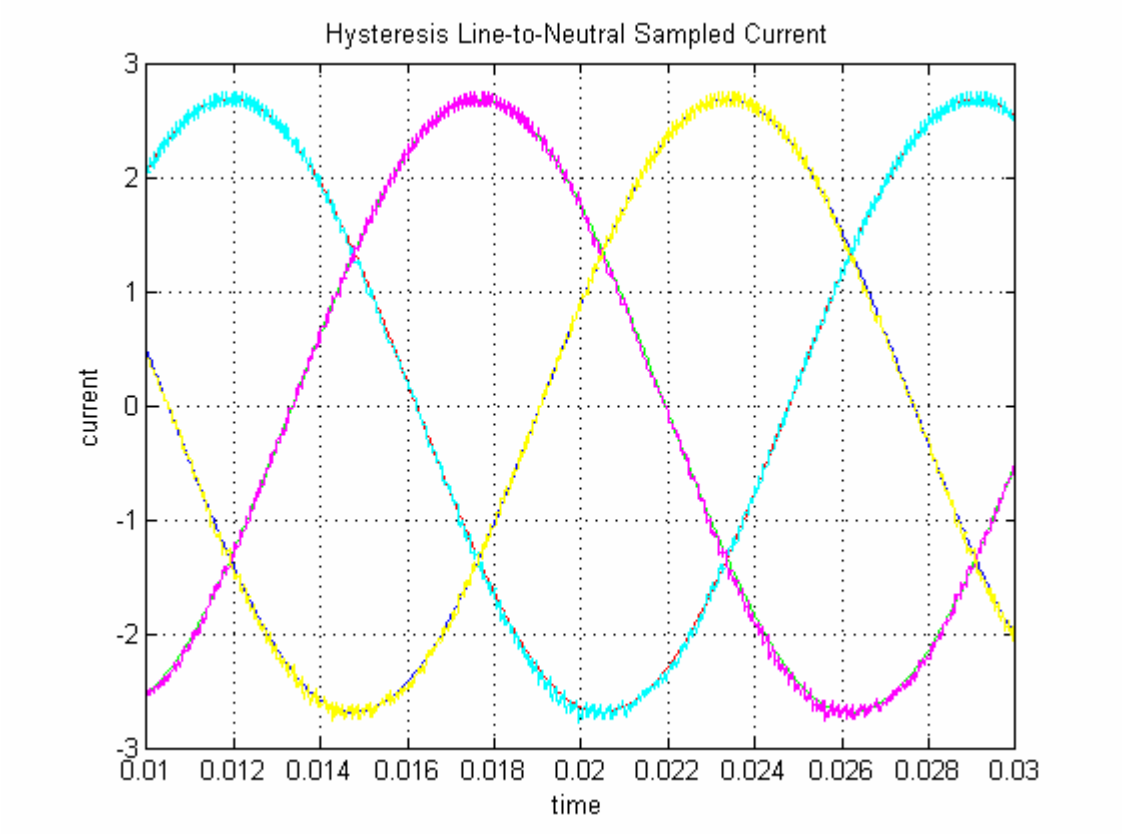

Figure 24 Three Phase Filtered Output

When using a six-step three-phase hysteresis controller, a switching event in phase-A could have an effect on the other two phases. Figure 25 is an enlarged portion of Figure 24. The arrows in Figure 25 show how switching events in the other phases effect the wave form of phase-A. One of the advantages of hysteresis control is its simplicity in implementation in that each phase can be controlled individually. This advantage far outweighs small non-uniform switching events which are theorized to effect even ordered harmonics.

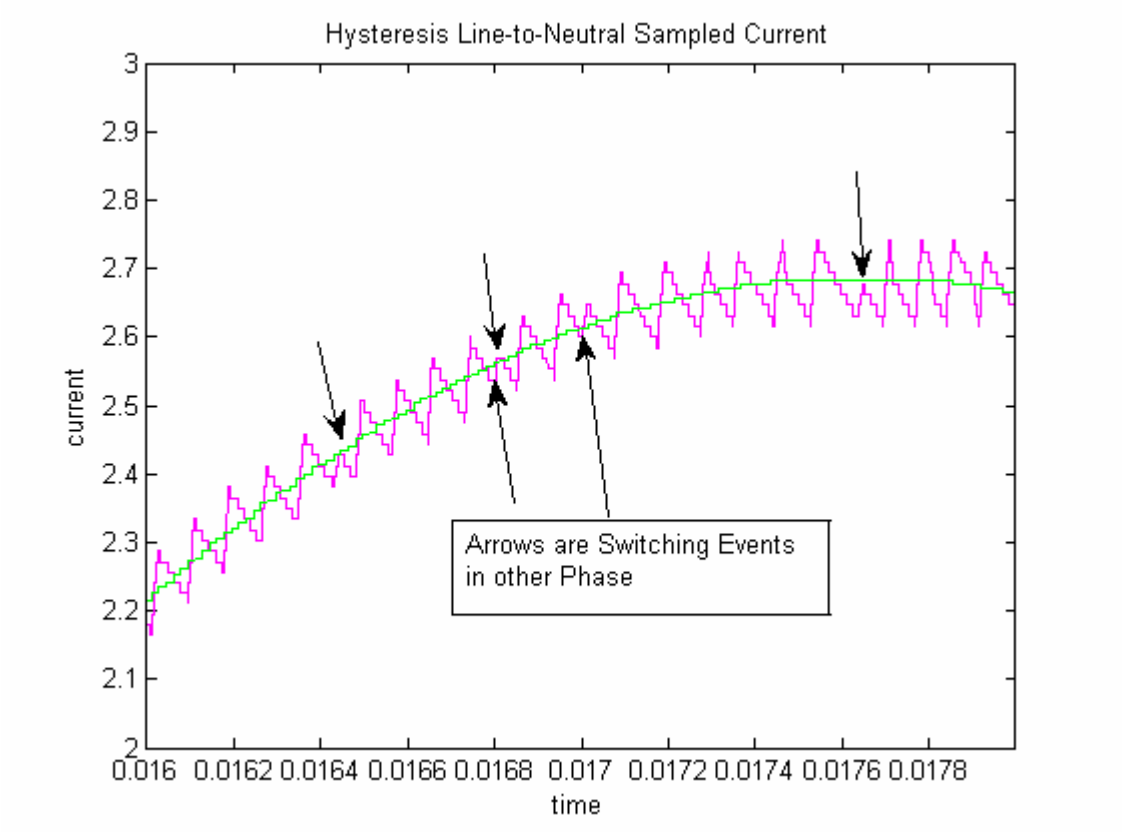

Figure 25 Switching Events

The harmonic of content of the filtered wave form is show in Figure 26. The odd harmonics that are not multiples of three which were the major contributor to the THD before have been essentially driven into the noise floor. The calculated THD of the composite output wave form is 2.27%. If the second, third and fourth harmonics are disregarded as suggested by theory, the THD becomes 0.748%. Essentially all of the harmonics have been driven into the noise floor and the energy has been spread evenly across the spectrum. The unexpected harmonics are mostly a reflection caused by proximity of the fundamental and other model anomalies. As will be seen, they are not present in the experimental results.

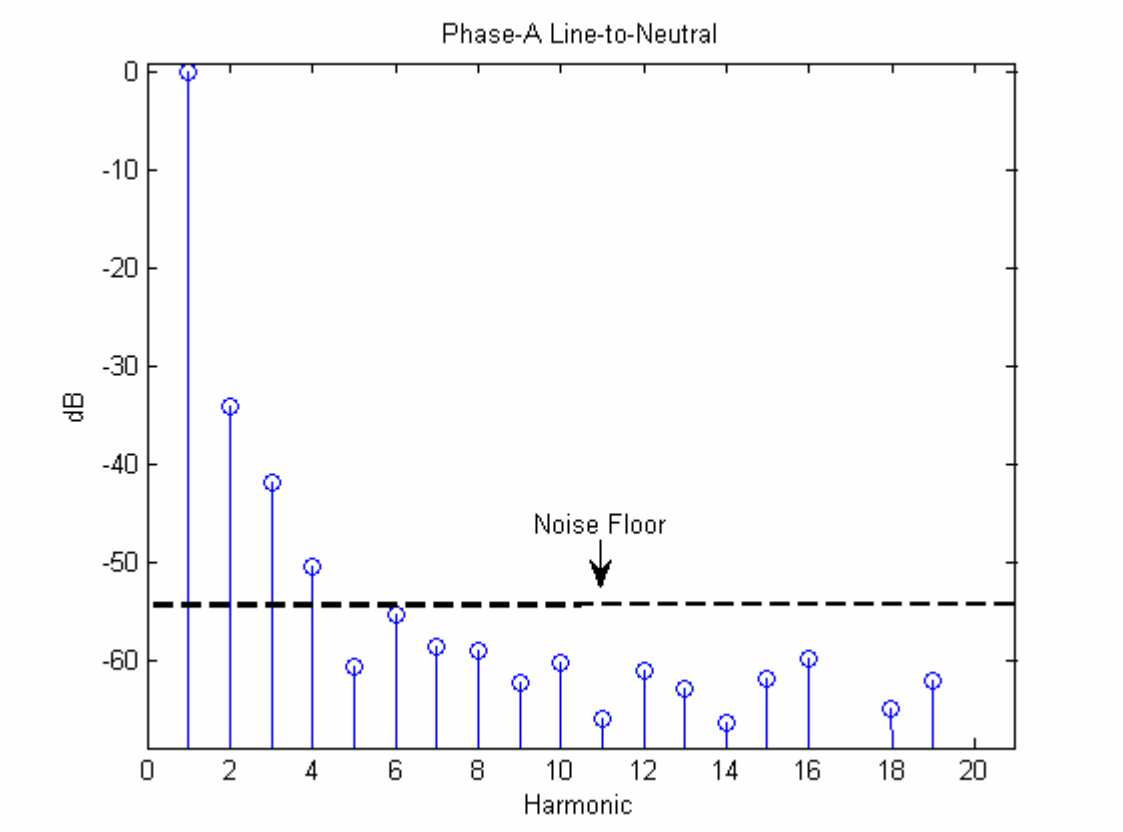

Figure 26 Total Current Harmonic Content

F. SUMMARY

The advanced tools of SIMULINK® allow modeling of the concepts and also the specific system hardware. However, it was rather difficult to find all the necessary time delays for accurate modeling results. The model predicts larger values for the second, third and fourth harmonics than anticipated based on mathematical calculations. Further work may be needed to refine the model. The model predicts a final THD of 2.27% or 0.748% based on inclusion or exclusion of the first three unexpected harmonics, respectively. Either way, this is below both navy and commercial limits.

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IV. HARDWARE IMPLEMENTATION

A. OVERVIEW

This chapter will outline the construction of the controller and hybrid inverter. The chapter consists of three major sections. The first section describes the load and associated isolation transformers. The second section clarifies the input inline reactors, the commercial PEBBs and the DC power source. The third section details the construction and implementation of control and sensing circuitry. Figure 27 is a block diagram showing the layout of the entire hybrid converter where *Load* section "---" (green), the *PEBB* section "– – –" (gold) and the *Control and Sensing* section "·· –" (blue) are highlighted.

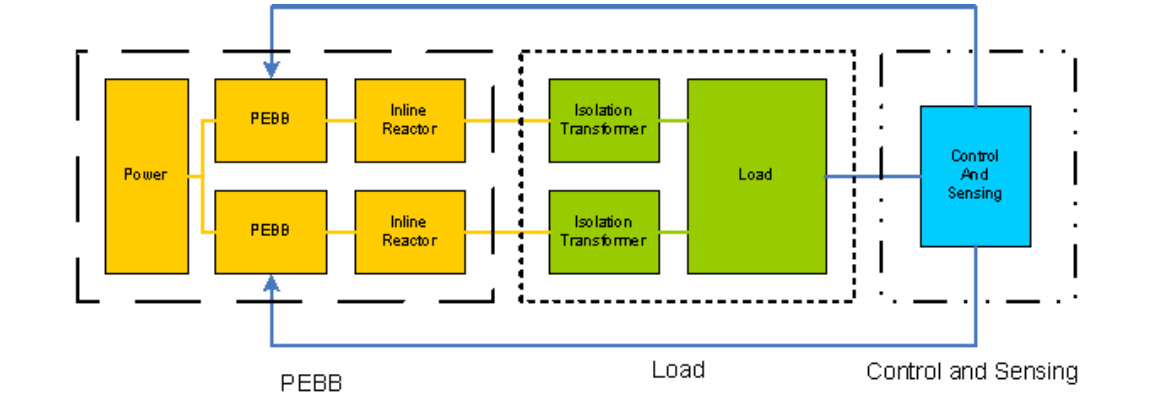


Figure 27 Project Block Diagram

B. LOAD

The *Load* section consists of resistors, reactors and transformers. Each phase of the wye-connected three-phase load consists of a 5Ω resistor in series with a 20mH inductor. The impedance of each phase is $9.05\angle 56.45°\ \Omega$. Figure 29 is a photo of the actual load excluding the isolation transformers.

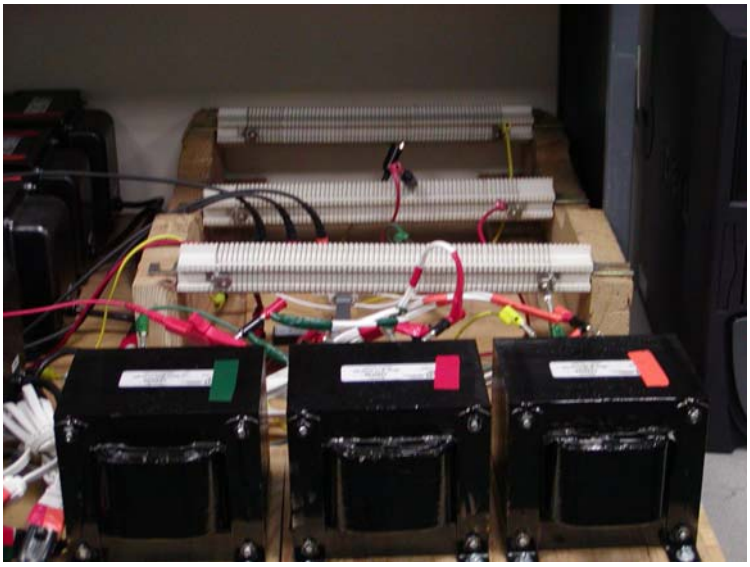


Figure 28 System Load

The load is separated from the *PEBB* section by two three-phase isolation transformers configured from six identical single-phase transformers as seen in Figure 29. Even though the impedance of each phase was within 5% of one another, a small zero-sequence current still existed. Further compounding this zero-sequence current was feedback control error. The isolation transformers were necessary to break the zero-sequence current loop and make the realization of the hybrid inverter easier.

Figure 29 Isolation Transformers

C. PEBB

The *PEBB* section consists of two identical three-phase inline conditioning reactors, two COTS PEBBs and one non-isolated DC power supply. There is a 2.5mH conditioning reactor between each phase of the PEBBs prior to entering the primaries of the six single-phase transformers (Figure 30). The main input DC power bus for the hybrid inverter is supplied by one power source while the controls are sourced with a small ancillary supply.

The conditioning reactors are necessary to prevent short-circuit current flow between the bulk inverter and the active filter. The most elegant solution combines the coupling reactors with the isolation transformers. However, readily available commercial components were used to create this function without the need for special order components. With a more refined system and with the necessity to increase power density, coupled reactors could be ordered.

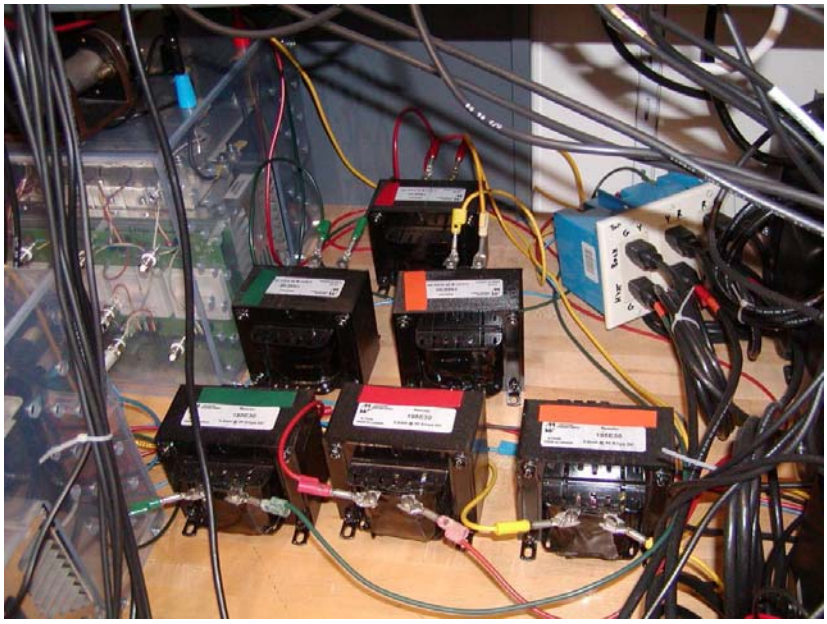


Figure 30 Conditioning Reactors

The PEBB is a Power Electronics Teaching System (PETS) manufactured by SEMIKRON and constructed with IGBT power semiconductors. The PETS is designed for demonstration purposes and thus mounted in a transparent Plexiglas package as seen in Figure 31. The schematic for the PETS is shown in Figure 32. There are three half-bridge modules in each PEBB consisting of two IGBTs with freewheeling diodes as

shown in Figure 32 (*S1-S2*, *S3-S4* and *S5-S6*). Each half-bridge is integrated as a type SKM 50 GB 123 D module. The gate driver that controls both IGBTs in each half-bridge is a SKHI 22B. This commercial driver offers the following built-in features:

- It provides galvanic isolation between the high voltage section and the controller card.
- It prevents simultaneous gating of upper and lower switches.
- It has short-pulse suppression where a gating pulse must be >500ns.
- It provides under voltage protection.
- It provides short-circuit protection through the monitoring of collector-to-emitter voltage.

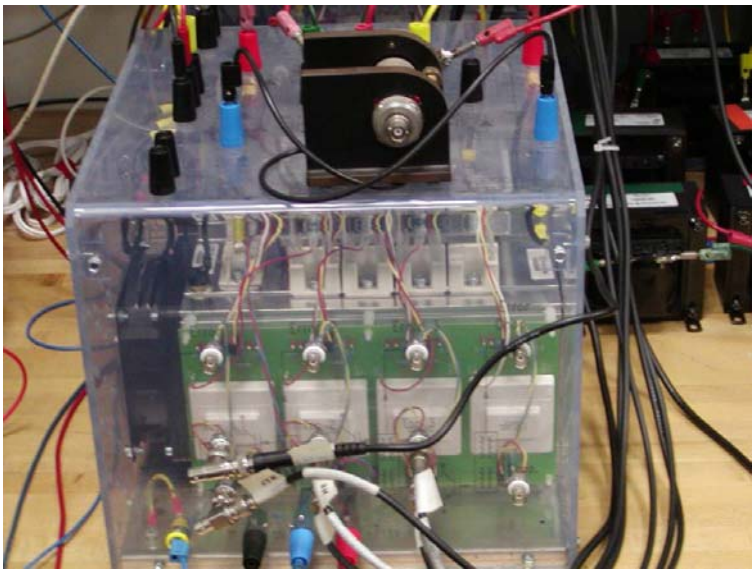


Figure 31 Power Electronic Building Block

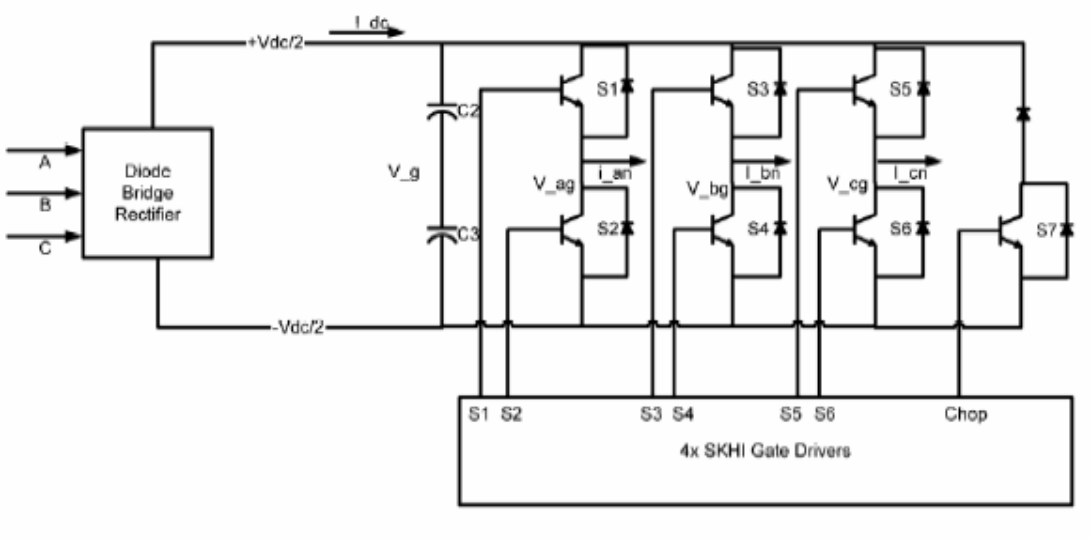


Figure 32 PEBB Schematic

[From Ref 13 above]

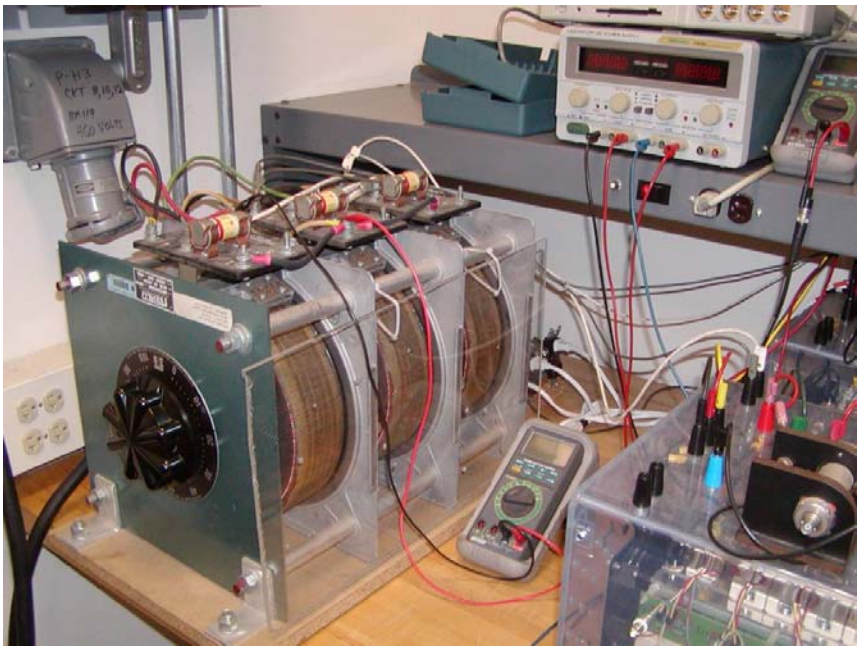


Figure 33 Three Phase AC Power Supply

The main power source for the system is supplied by a 480V 60Hz 33.9kVA three-phase variac with a diode bridge and filtering capacitors (see Figure 33). The diode bridge and filtering capacitors are inside each of the PETS. Ancillary power for the PEBB driver cards is supplied by a Tektronics PS280 DC power supply set to 15 V.

D. CONTROL AND SENSING CIRCUITRY

The *Control and Sensing* section consists of an FPGA development kit, an interface card, the software interface and a Hall effect sensing card. This thesis leverages previously presented material on parallel hybrid inverters in NPS theses with the use of an entirely new controller hardware.

1. Development Kit

A Virtex-II™ development kit was purchased from MEMC™ Corporation. The development kit was designed to be an easy to use developmental platform for prototyping and verifying designs. The block diagram of the major functional components of the Virtex-II™ development kit is shown in Figure 34. The kit utilizes the XILINX® XC2V1000-4FG256C FPGA. There is an ISP PROM on the board that allows the program to be stored and loaded during start-up or when the *PROG* switch (reset) is depressed. The JTAG connector is used as a port to load the software from a PC. Even though there are several clocks available, the default runs at 100MHz. The 5.0V connector pin is used to supply the main power to the card. All other card power is derived from this 5.0V input. The rest of the power options were not used for this project. The Virtex-II™ development kit has two 64-pin interface connectors labeled *J11* and *J12* (Figure 35). These connectors provide easy access to the NPS interface card.

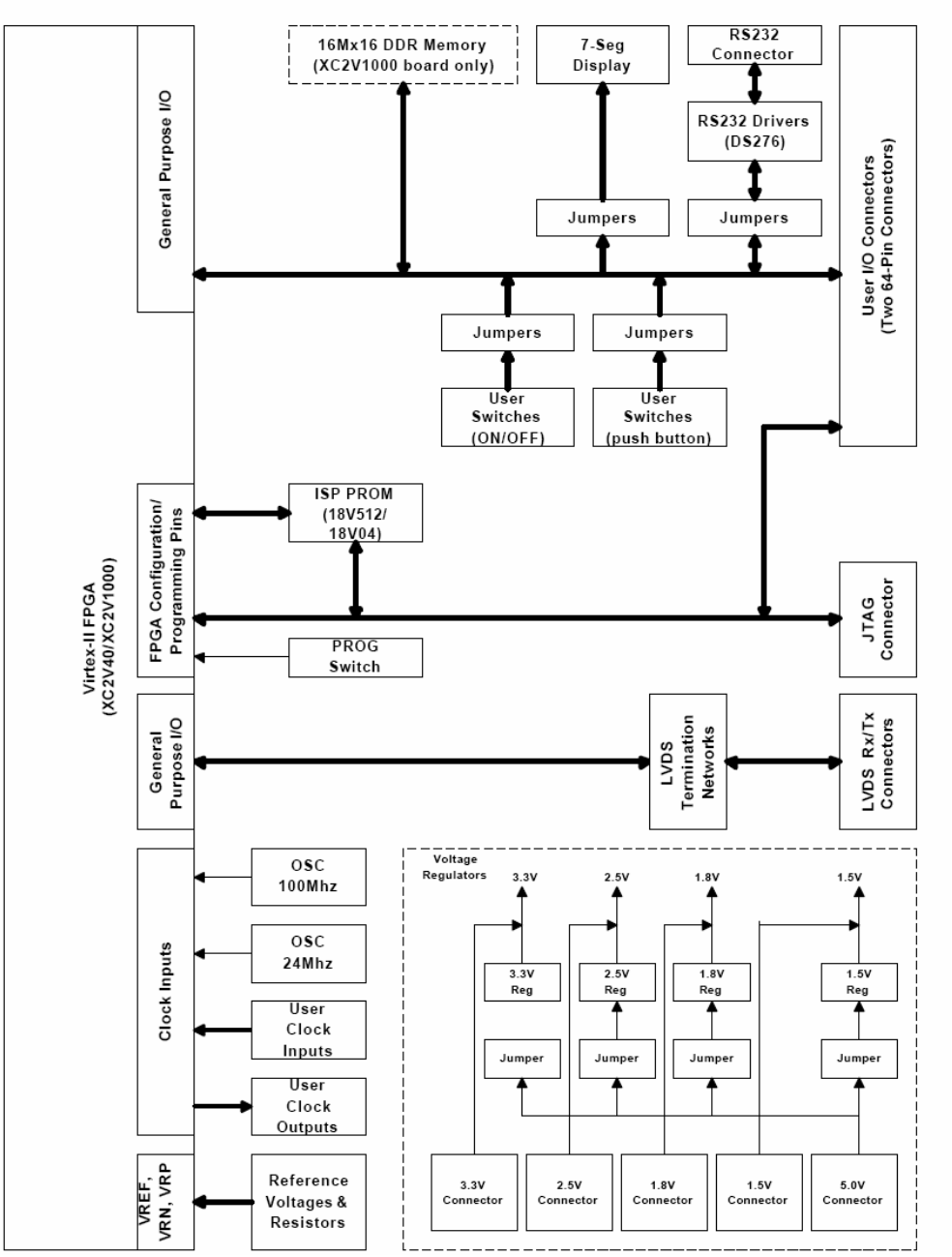


Figure 34 Virtex-II^{TM} Development Kit Block Diagram

[From Ref 16]

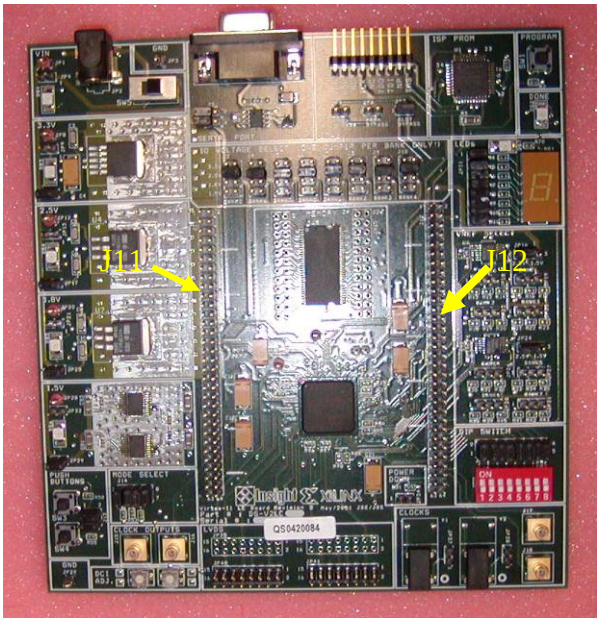


Figure 35 Virtex-II™ Development Kit

2. NPS Custom Interface Card

The interface card was designed to bridge the gap between the Virtex-II™ development kit, the SEMIKRON PEBBs and the Hall effect sensors. The interface card performs the following functions:

- It supplies 5V power to the Virtex-II™ development kit.
- It level shifts the low voltage gate driver signals from the development kit (0 – 1V) to the proper level for the PEBBs (0 – 15V).
- It contains an interface to the development kit.
- It provides 12 BNC connectors for the gate signals to the PEBBs.
- It provides an A/D converter to receive input signals from the Hall effect sensors.
- It provides test points for troubleshooting.

After outlining these required functions, components were identified for each need. Additionally, four extra output connections were added for future projects. This permits multiple cards to interface with each other. The interface card was designed using a software package that allows quick design implementation of multi-layer boards (PCB123®). The complete card layout, schematic and Bill-Of-Materials (BOM) is included as Appendix B. The final four-layer card has an inner digital and analog ground

plane layer, an inner power plane layer, a top signal layer and a bottom signal layer. The bottom of the card contains the Virtex-II™ interface connectors and the top of the card contains the rest of the components and connectors. The combined layout is shown in Figure 36. Six boards were ordered at a cost of $67 each and are shown as Figure 37. Two of these boards were populated and successfully tested. Figure 38 shows the completed interface board installed in the system with all of the connections wired.

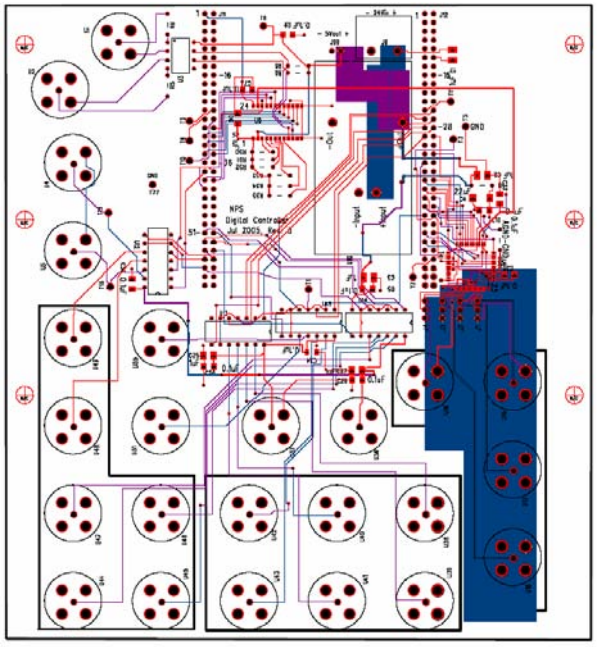


Figure 36 Interface Board PCB123 ® layout

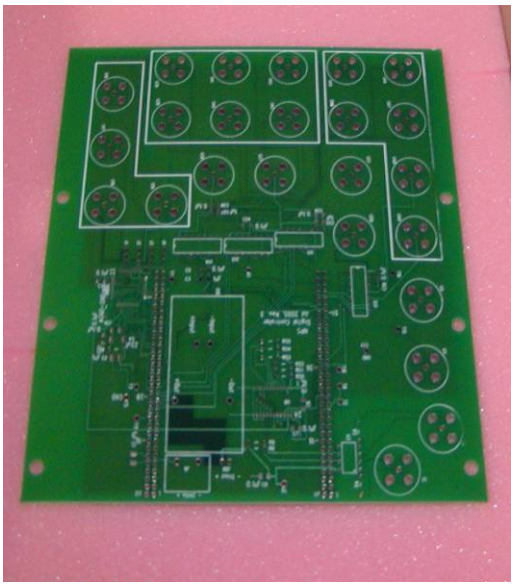


Figure 37 Printed Interface Board

Figure 38 Interface Board Completely Connected

3. Software Interface

The block diagram for loading the software from the computer to the FPGA is shown in Figure 39. The JTAG cable with appropriate blue colored jumpers is shown in Figure 40. The jumper placement is documented in Appendix C. One of the primary reasons for choosing the XILINX® family of development kits was the ability to perform the software engineering in MATLAB's SIMULINK® rather than programming in a low level Hardware Description Language (HDL) of an FPGA.

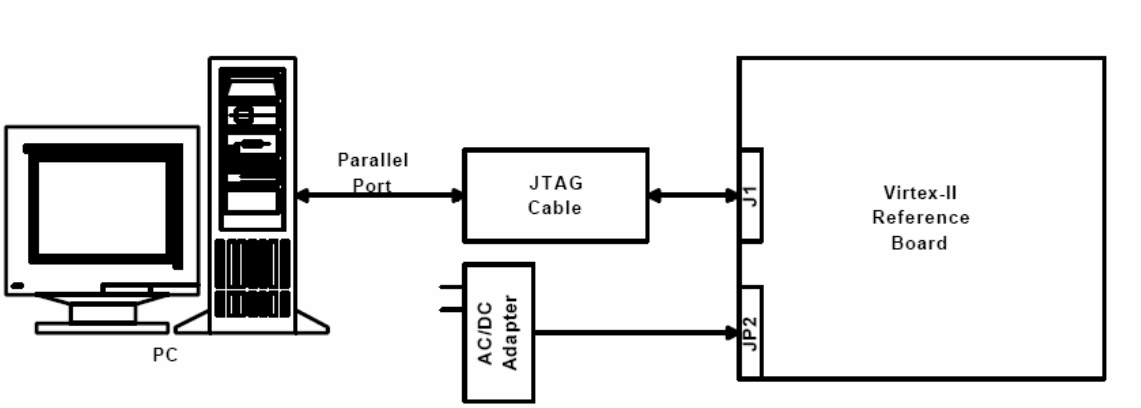


Figure 39 Software Interface Block Diagram
[After Ref 16]

Figure 40 JTAG Cable

The SIMULINK® models developed in the previous chapter modeled the entire system including all hardware. The SIMULINK® models which included the XILINX® block set are than converter to Hardware Description Language (HDL). Once the HDL code is obtained, it is converted to a netlist which must be subsequently verified in a follow-on step. This is done using *XILINX® Project Navigator* as shown in Figure 41. The project navigator allows the netlist to be compiled into a form that can be directly loaded into the FPGA or the ISP PROM. The project navigator also reports on the percentage of the FPGA usage. For this thesis, only 21% of the total FPGA was required for the program.

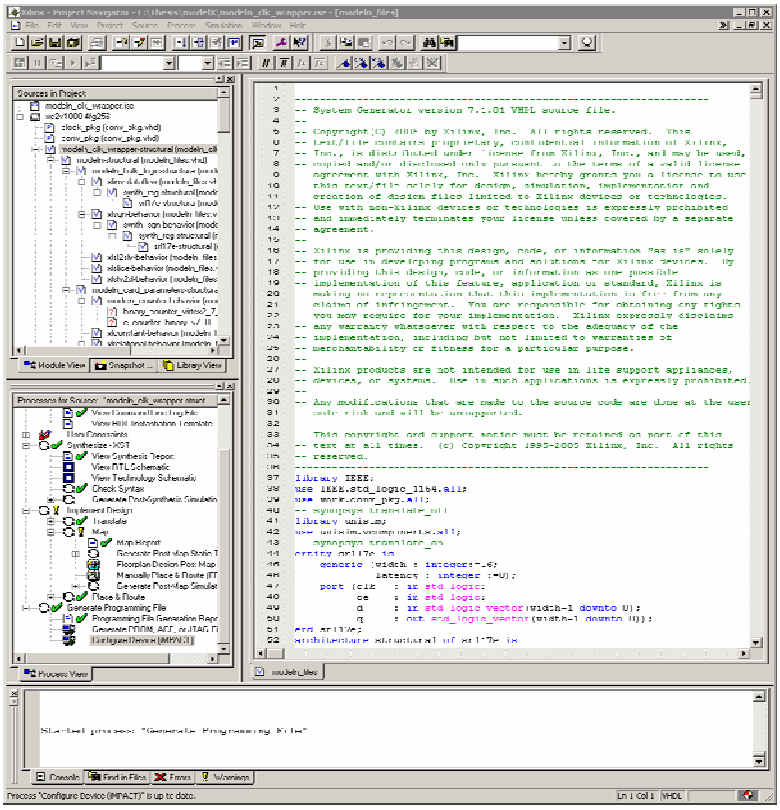


Figure 41 XILINX® Project Navigator

After verification, the netlist can then be fitted to the FPGA using a process called place-and-route. The place-and-route process is done by *XILINX® iMPACT*. The graphical interface is very easy to use by right-clicking on the icon and selecting the appropriate file to load.

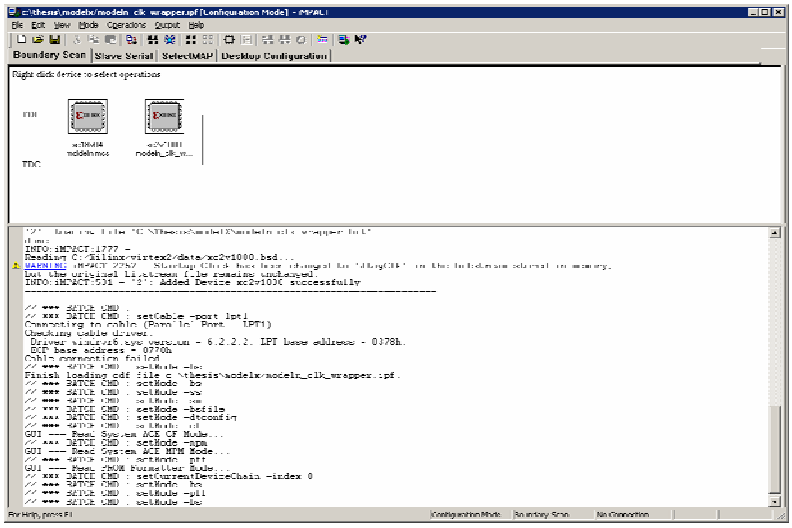


Figure 42 XILINX® iMPACT™

4. Hall Effect Sensors

The controller requires input currents from each of the three phases of the load. The Hall effect sensor module was built using three FW Bell CLN 50 HES. The circuit was constructed directly from an FW Bell application note. A dual-output DC-DC converter was used to convert 24VDC to ±15VDC to power the board. The card layout is shown in Figure 43 while the complete schematic is contained in Reference [6].

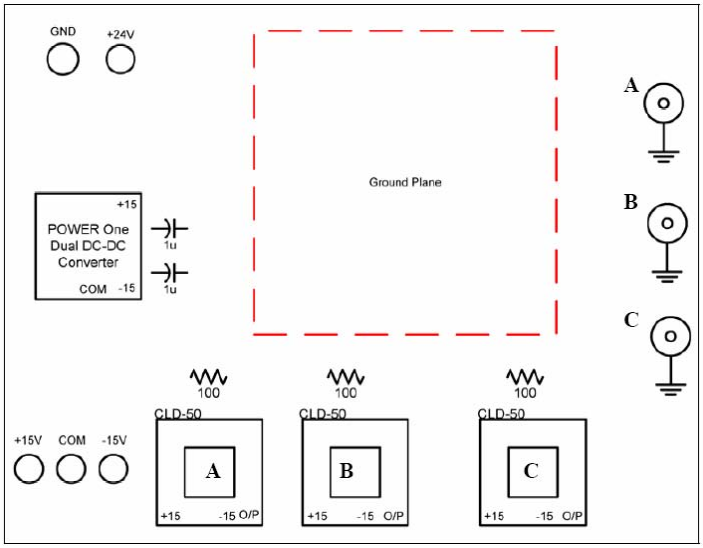


Figure 43 Hall Effect Sensor Layout
[After Ref 6]

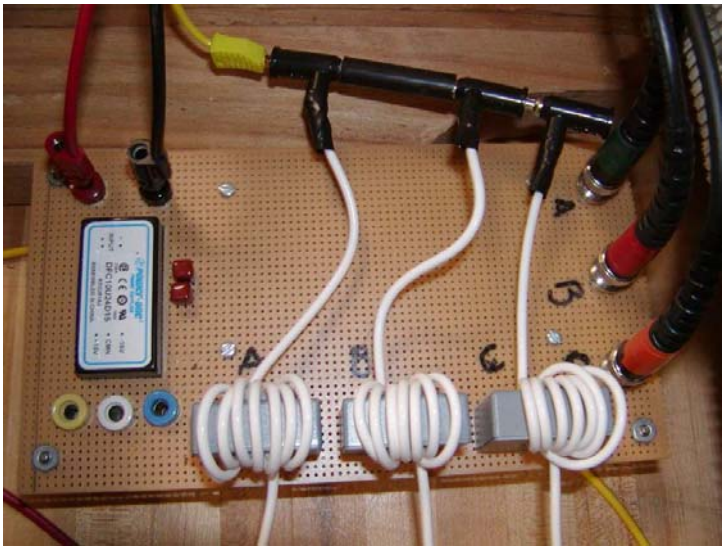


Figure 44 Hall Effect Sensor Card

E. IMPLEMENTATION

The complete set up including monitoring equipment is show in Figure 45. Two Tektronix PS280 variable power supplies set to ±15VDC were used to power the PEBB driver cards and the combine NPS interface card with Virtex-II.™ An HP 3561A Dynamic Signal Analyzer was used to measure the frequency spectrum for the output current of each phase. Three Tektronix TDS 3012B scopes were used to monitor various test points via Tektronix P5205 differential voltage probes and TCP202 current probes.

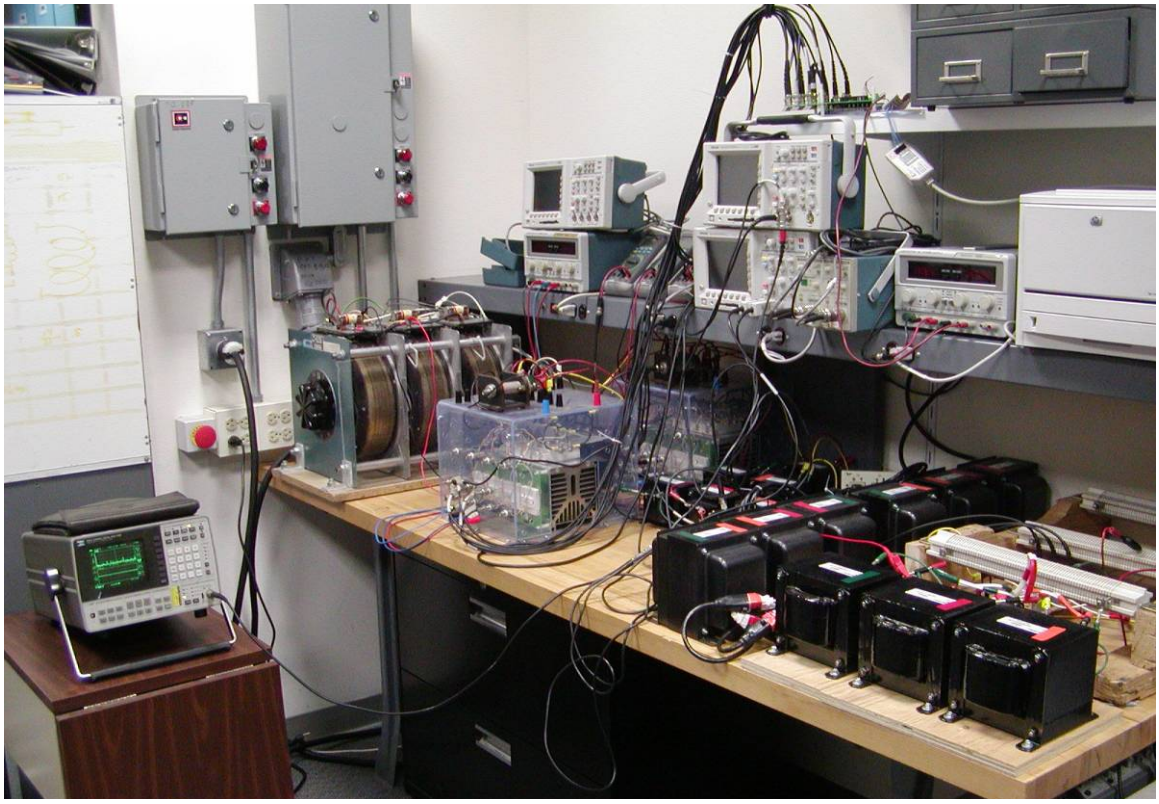


Figure 45 Complete Set Up

F. SUMMARY

This chapter discussed the construction and assembly of the hybrid inverter system. The heart of this project was the NPS controller card and the development kit. The current configuration only uses about one-quarter of the potential of the FPGA. This low utilization allows for expansion of the system well beyond the existing level. The next chapter will discuss the experimental results.

V. EXPERIMENTAL RESULTS

A. OVERVIEW

This chapter presents the testing results of the NPS custom interface card, the six-step bulk inverter and the entire hybrid system.

B. NPS CUSTOM INTERFACE CARD TESTING

After receiving six unpopulated Printed Circuit Boards (PCB), testing began with point-to-point continuity checks of all the traces. This revealed one bad card. The two good cards were then populated and rechecked for continuity problems. Power was then applied to the boards and all available test points were checked for proper voltage levels. The NPS custom interface card was then mounted on the Virtex-II^{TM} development kit, powered, and tested at select test points. The development kit is very sensitive to static discharge and short-circuits as was witnessed in previous projects. Therefore, monitoring was limited to push-pin sites on the PCBs to prevent damage. The computer interface was tested by connecting the JTAG cable, powering the card and running the iMPACT program. If the iMPACT program finds the FPGA on the Virtex-II^{TM} card, the controller is ready for programming. A functional check of the interface was completed by uploading a simple program into both the FPGA and the ISP PROM. Further, the BNC outputs were checked by uploading a program that produced a 60Hz square-wave signal. Several cold solder joints on the level-shifters were corrected during these tests. The final test of the controller incorporated the A/D converter. A 20KHz sine wave was injected into each input channel, the digital steam was sent to each of the output channels, and each output channel was connected to an external D/A converter for signal recovery.

C. SIX-STEP BULK INVERTER TESTING

The first test produced the reference wave forms required to drive the three-phase six-step bulk inverter described in Chapter II, Figure 5. The desired gate signals for the upper transistors of the bulk PEBB as obtained from the NPS interface card can be seen in Figure 46. The lower transistor signals are the exact inverse.

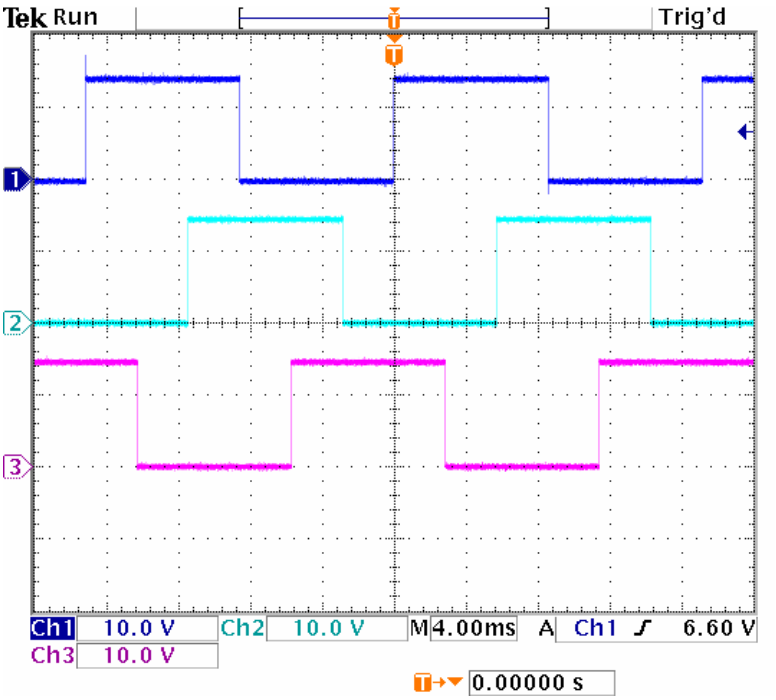


Figure 46 Gating Signals

Figure 47 displays the phase-A line-to-line output voltage with no load. The expected results were presented in Chapter II, Figure 6.

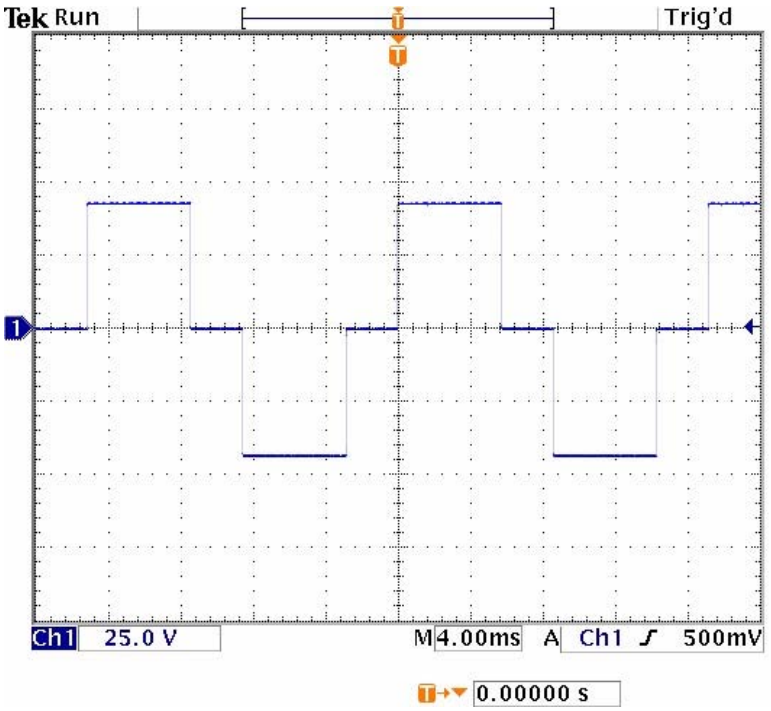


Figure 47 Phase A Line-To-Line

Figure 48 shows the phase-A line-to-neutral output voltage with a purely resistive load and no in-line reactors. The modeled results were presented in Chapter II, Figure 7.

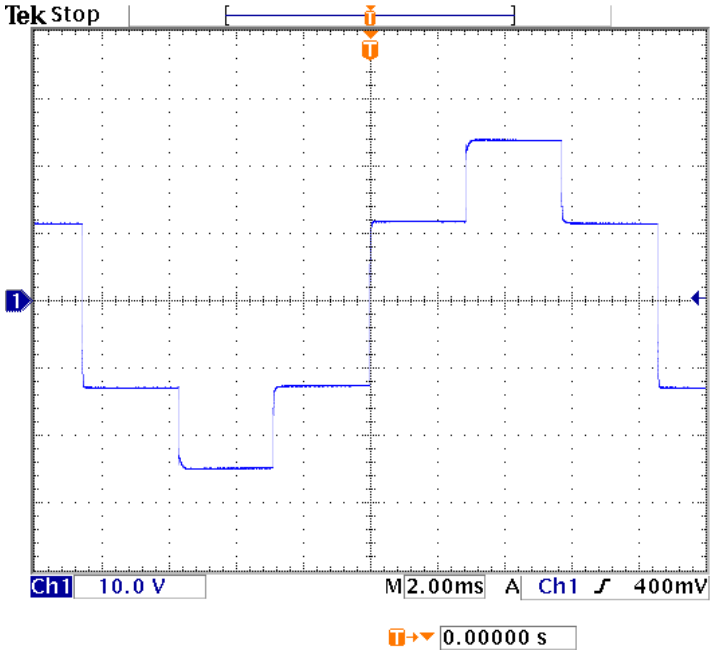


Figure 48 Phase A Line-To-Neutral

The phase-A line-to-neutral wave form for voltage and current is shown in Figure 49. This matches the predicted wave form from Chapter II, Figure 9.

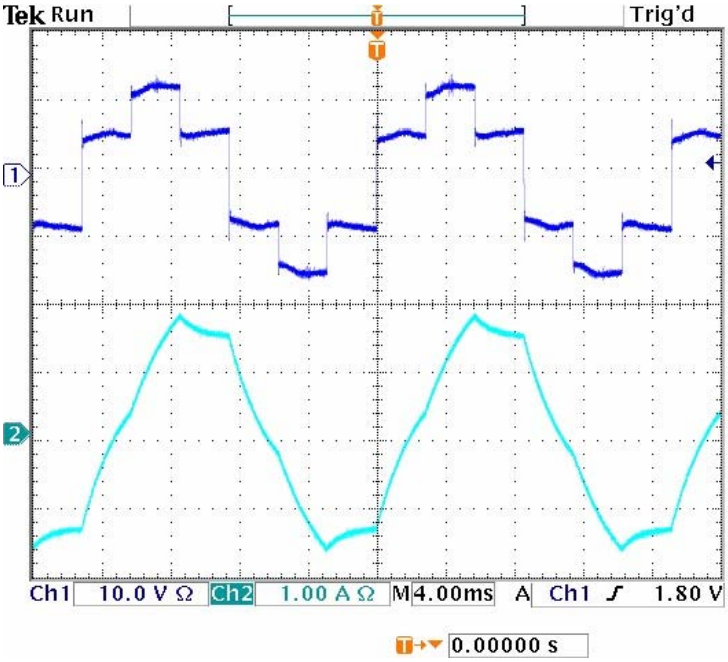


Figure 49 Phase A Line-To-Neutral Voltage and Current

Figure 50 shows the three-phase line-to-neutral current of the six-step bulk inverter. This matches the modeled results in Chapter III, Figure 22.

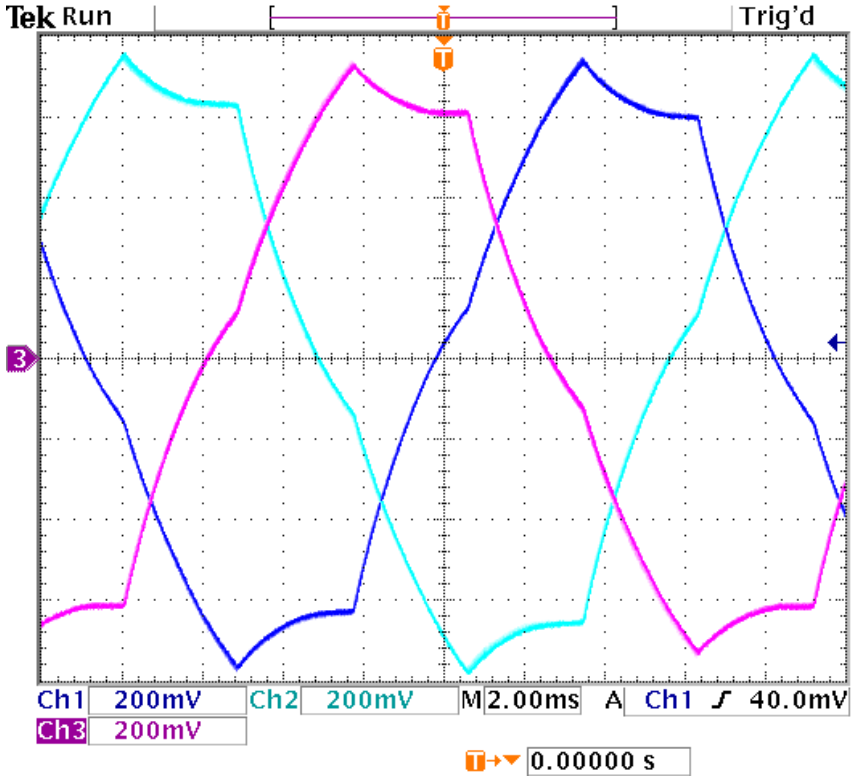


Figure 50 Bulk Inverter 3-Phase Line-To-Neutral Current Wave Form (200mA/div)

The SIMULINK® model presented in Chapter III, predicted a current THD of 7.5% using the first 20 harmonics. Using the first 20 harmonics of the line-to-neutral current for phase-A, the HP 3561A Dynamic Signal Analyzer calculated a THD of 7.5%.

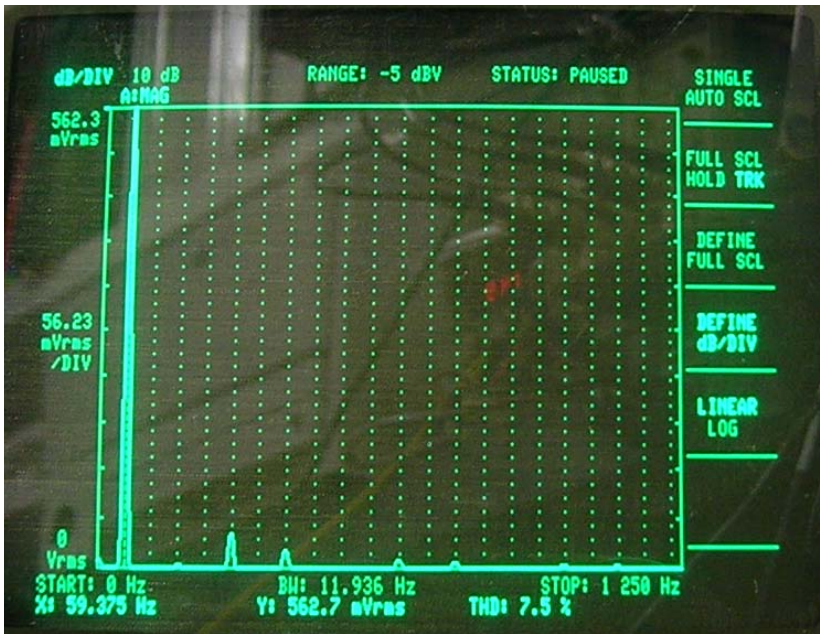


Figure 51 Spectrum Six-Step Line-To-Neutral Current

By plotting the frequency spectrum for the line-to-neutral current signal, the largest harmonic with respect to the fundamental is the fifth at –23.2 dBV (Figure 52). This correlates with the modeling results of –25.8 dBV shown in Figure 23 of Chapter III.

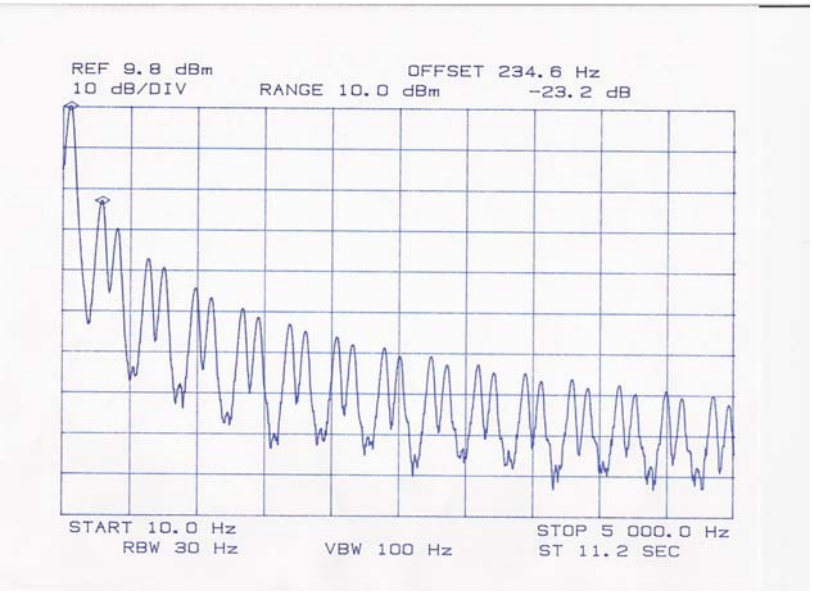


Figure 52 Line-To-Neutral Bulk Current Harmonics

The predicted results from the theory in Chapter II and the models from Chapter III of the six-step inverter are consistent with the measurements performed on the actual hardware.

D. HYSTERESIS CONTROL RESULTS

In order to initiate harmonic correction, the hysteresis inverter must be activated or engaged. With the hysteresis controlled active filter engaged, the current wave forms in Figure 50 become the sinusoidal wave forms shown in Figure 53. This matches the modeled results from Chapter III, Figure 24.

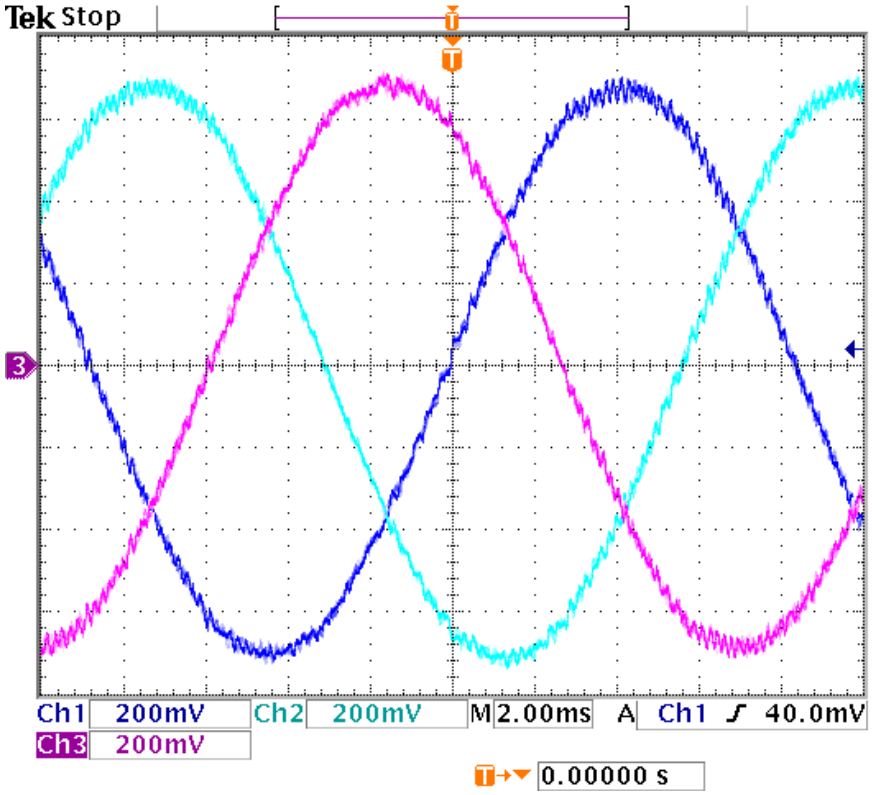


Figure 53 Three Phase Line-To-Neutral Hysteresis Filtered Current

The composite line-to-neutral voltage and current for phase A are shown in the upper and lower portions of the display of Figure 54 respectively. It is apparent that the voltage wave form is ridden with high frequency switching action from the hysteresis controlled

active filter. However, the load inductance is quite effective in filtering the high frequency hash as is apparent in the current wave form.

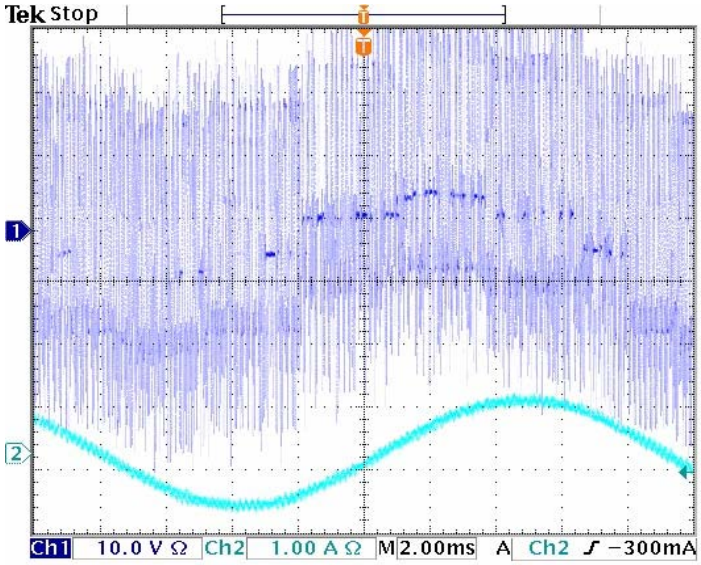


Figure 54 Line-To-Neutral Voltage and Current with Hysteresis Controlled Active Filter

The 3561A Dynamic Signal Analyzer calculated a THD of less than 1% using the first 20 harmonics (Figure 55). This correlates well with the 0.75% phase-A current THD from the modeling data.

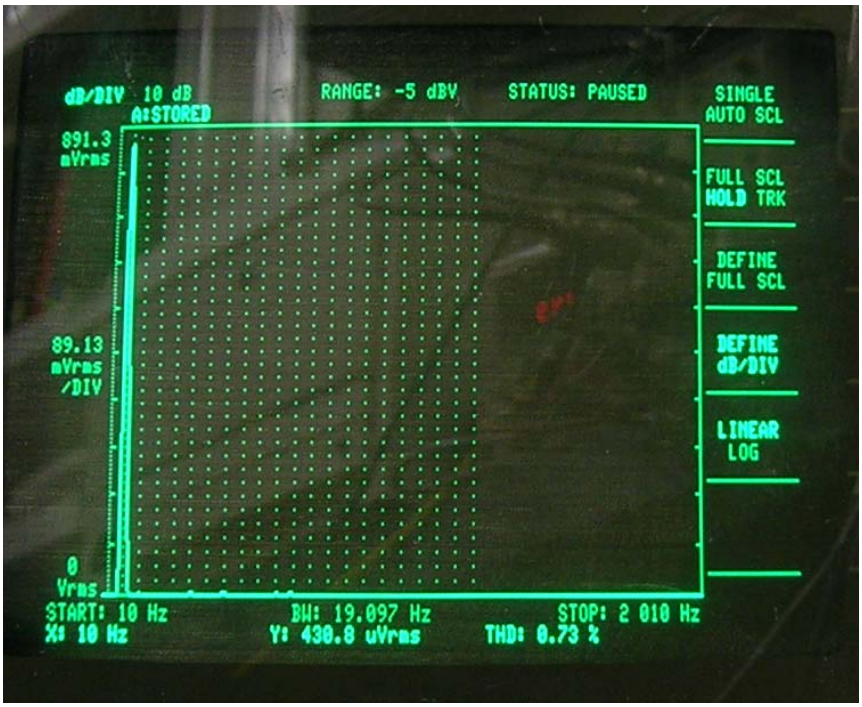


Figure 55 Line-To-Neutral Current Spectrum with Hysteresis Filter

The fifth harmonic is –48.4dBV below the fundamental and is in the spread-spectrum noise floor as seen in Figure 56. This is an improvement of more than 25dBV when compared to the six-step inverter (Figure [53]). However, this is not quite as good as the modeling results of –53dBV shown in Figure 26 of Chapter III. The hysteresis control method also has the effect of spreading the harmonics over the entire spectrum. This is considered an advantage over typical Pulse Width Modulation (PWM) techniques that produce specific tonals trackable by sonar. It does have the disadvantage of raising the noise floor as seen by comparing Figure 52 and Figure 56.

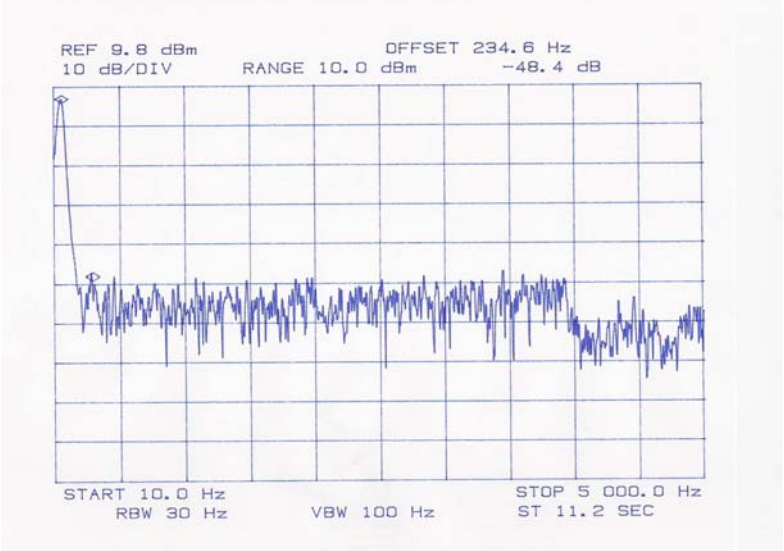


Figure 56 Line-To-Neutral Current with Hysteresis Controlled Active Filter

E. OBSTACLES

This section presents the obstacles, the temporary solutions and future resolutions. There were two obstacles to transverse during hardware testing:

- The isolation transformer internal breakers would trip even though the output current was well below the 10A rating. This may be due to the high frequency ripple current of the hysteresis inverter or the additive effect of the coupled system. Either way, the analysis was left for a future student. The problem was circumvented by simply reducing the system input voltage to 50V from 100V.
- Additionally, the system was found to be unstable at the point where the hysteresis inverter produced additive fundamental current. This is believed to be a phenomenon of the existing control philosophy which relies on a modeled or expected impedance. This anomaly can be corrected in a future iteration of the software by monitoring and using the actual output current wave form of the bulk inverter to generate the hysteresis reference wave form. However, to overcome this issue, the hysteresis inverter was always programmed to subtract a small portion of the fundamental current from the bulk inverter. Ideally, the hysteresis inverter should only produce harmonic current and not fundamental.

F. SUMMARY

This chapter presented the results from testing the NPS interface card, six-step bulk inverter and the system with the hysteresis controlled active filter engaged. The next chapter will discuss conclusions from testing.

VI. CONCLUSIONS

A. OVERVIEW

This chapter will present some conclusions from this research project and suggest several areas for future study.

B. CONCLUSIONS

This thesis successfully completed the stated objectives below:

- A model was generated using SIMULINK® that included both the parallel hybrid concept and the hardware used to implement the concept. The model predicted the behavior of the system accurately with the exception of numerical errors that incorrectly included even and third ordered harmonics in the output of the inverter system. This is probably due to the non-symmetrical nature of the hysteresis controlled active filter. A future investigative effort will need to be done in order to refine the model to more accurately reflect the known absence of these harmonics.
- A custom interface card was designed, constructed and tested to allow the use of an FPGA to control two COTS PEBBs.
- The final resulting line-to-neutral sine wave THD was less than 1% which is below the Navy and IEEE limits.

Successful testing of the controller has validated the efficacy of the system. This type of system could be used in the powering of propulsion sized motors in future naval applications. Laboratory results showed that the hysteresis controlled active filter is capable of reducing the THD well below the Navy and IEEE standards.

C. FURTHER STUDY

There are several areas that could be pursued as future thesis work at NPS and they include the following:

- Further refinement of the initial model created in SIMULINK® that more accurately reflect laboratory results will need to be generated. One identified area of non-symmetrical wave form generation is timing delays introduced by the modeled A/D converter.
- The control strategy can be expanded to include variable frequency output by hooking up an actual motor and closing the speed control loop.

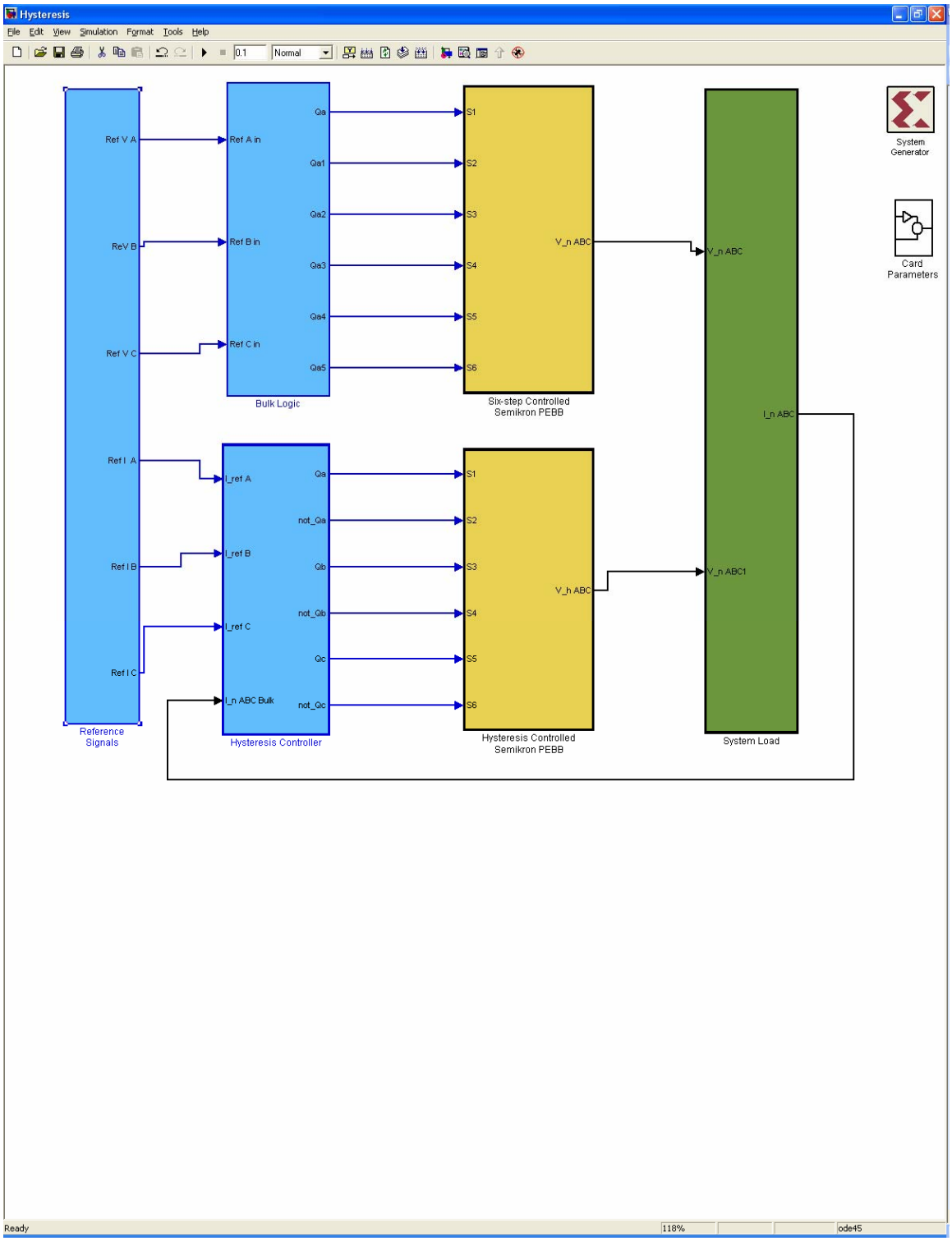
- The control strategy can be expanded to include a variable DC power supply on the front end. The NPS control card has an additional A/D channel that could be used for this purpose.
- The control strategy expanded to include the measurement of the zero-sequence current. This current should be targeted for elimination in order to eradicate the use of bulky 60Hz isolation transformers.
- The hysteresis controls can be shifted into the quadrature-direct-zero (qd0) reference frame and further optimized [9].

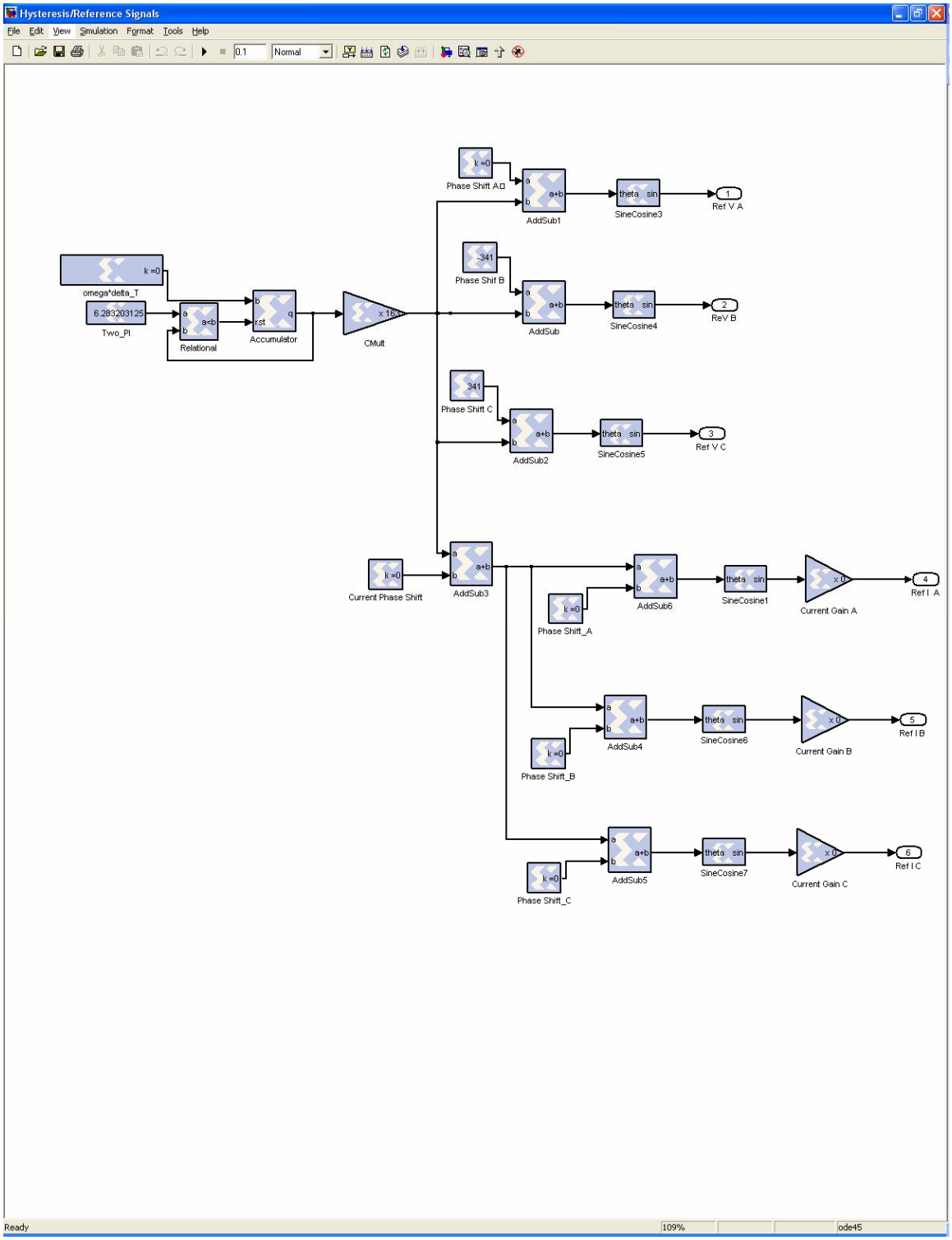
APPENDIX A. SIMULINK® SCHEMATICS AND MATLAB® CODE

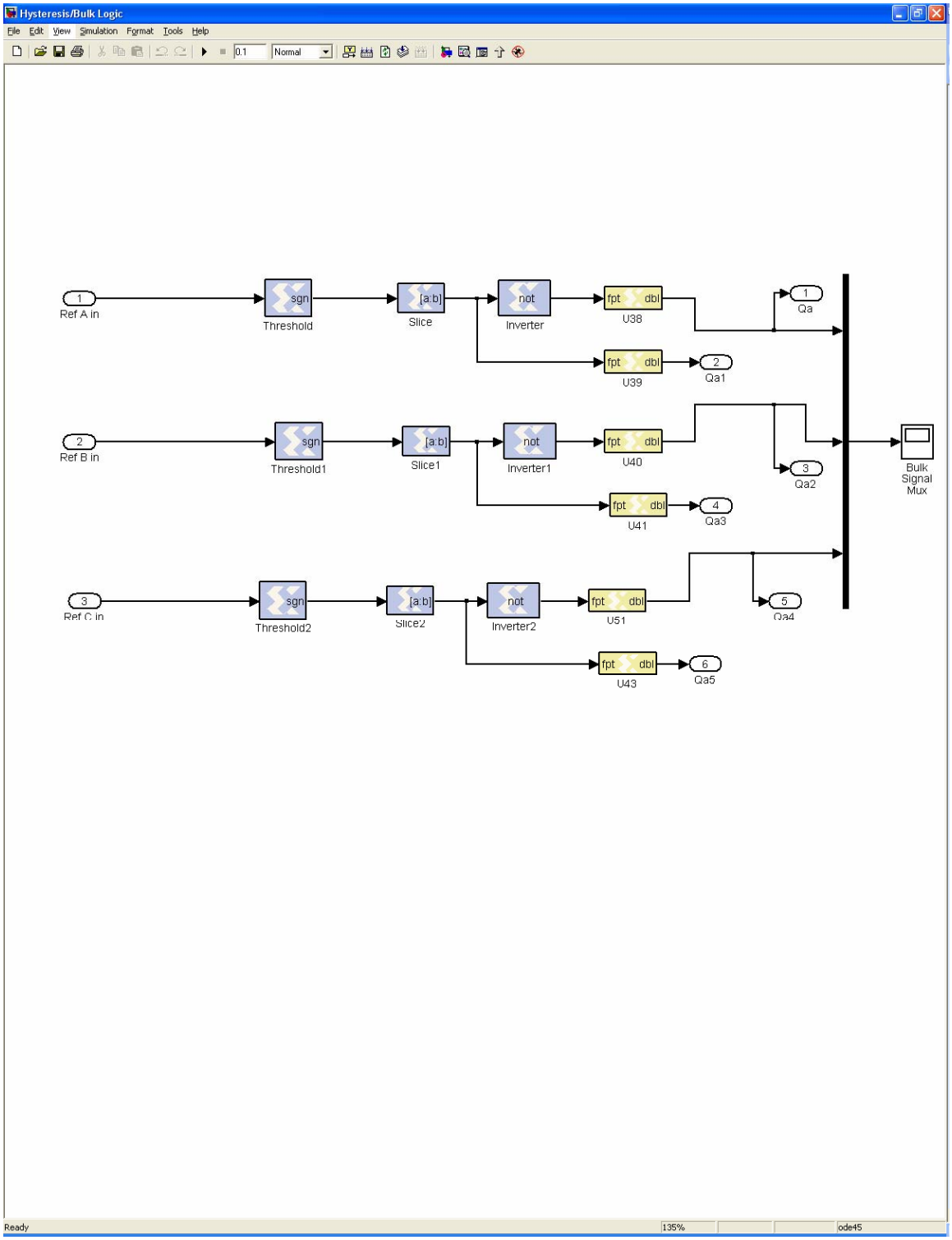
A. SIMULINK® MODEL INITIALIZATION M.FILE

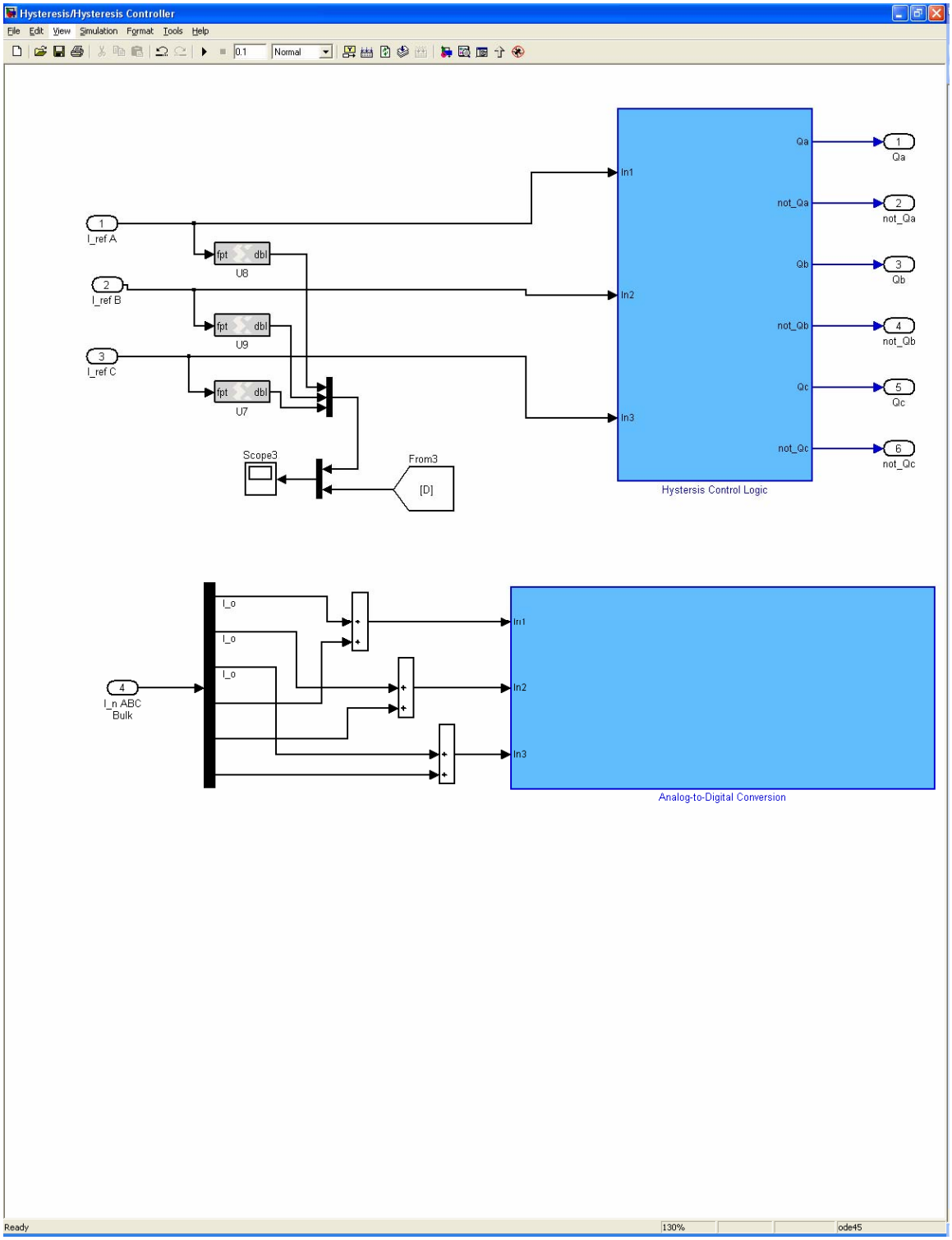
```
%Init file for Matlab® Model with Xilinx® commands
%John Lund Thesis
clear
 clc
Vdc = 50;
%***** Load resistance and inductance values *****

%***** coupling inductors *****
L_c = 2.5e-3; %mHenrys
R_c = 0.025; %Ohms (worst case assumed)

%***** RL load *****
L_l = 20e-3; %mHenrys
R_l = 10; %Ohms

%***** Issolation transformer *********
L_i= 10.2e-3;

%***** Fundemental Frequency ***********
f_fund = 60;

%***** Calculations and constatnts set ********
R=R_l+R_c;
Lh=L_l+L_c+L_i;
Lb=L_l+L_c+L_i;
Z=R+2*pi*f_fund*Lb*i;
I=1/Z;
ph=angle(I);   % ** Used to set phase difference

mag1=abs(Vdc*2/3/Z)*sqrt(3)
% ****** A to D parameters *****************
F_mat = [0 0 0 1;1 1 2 0;2 2 3 0;3 3 0 0];
O_mat = F_mat;
step_ct=1;
tstep = 1/24000000*step_ct;
dtobfactor=10/4096/2;
AtoDadjust=409.6;
% *******  Hysterisys parameters************
delta_h = 0.05;

% ************ Gain adjustments for measuring devices *********
Gaininmodel=10*2^(8);

% *********** Phase shift for delta to Y connection **********
psft=-171;

% scope points
N=5000;
```

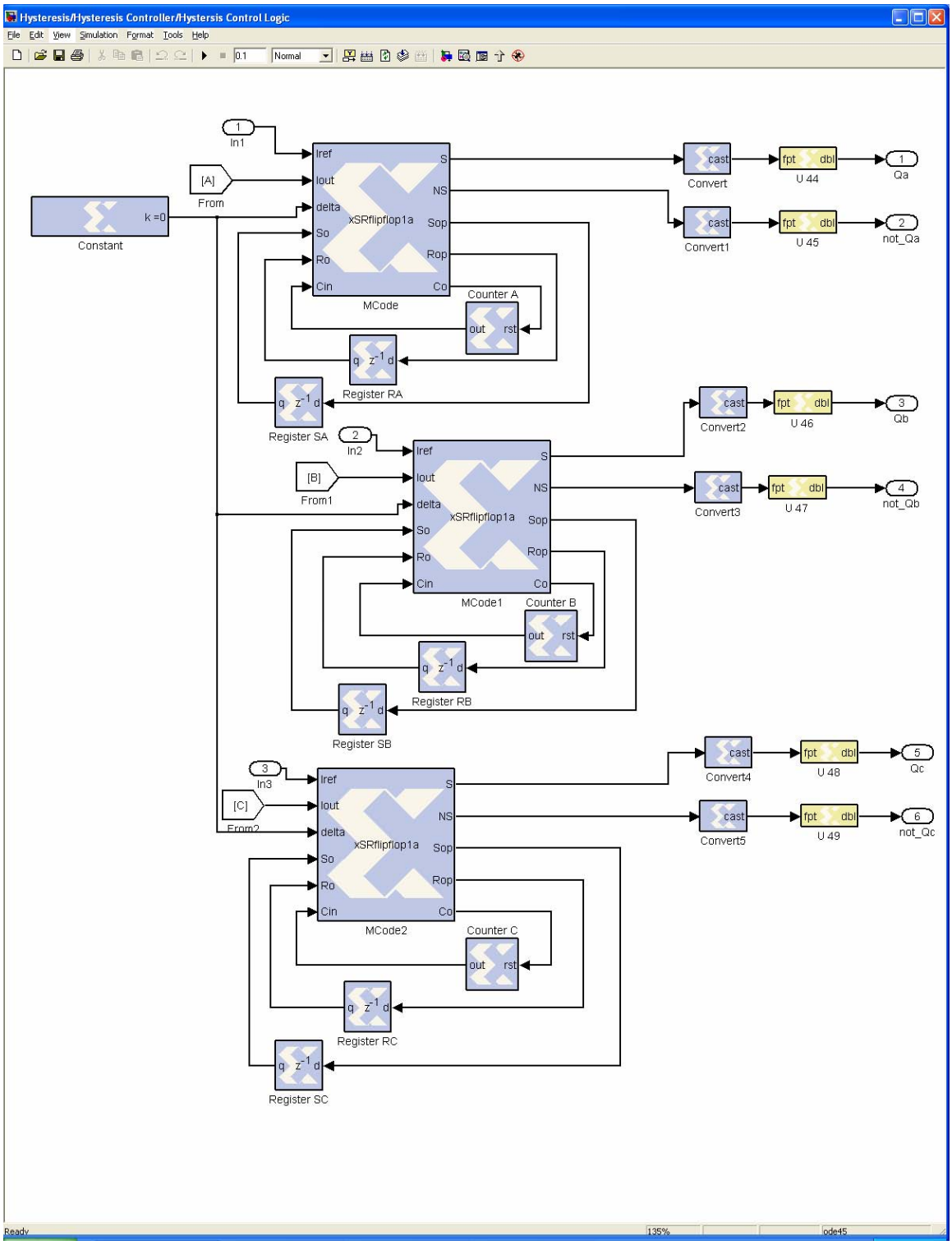
B. SIMULINK® SCHEMATICS




Hysteresis/Reference Signals
File Edit View Simulation Format Tools Help
Normal
Phase Shift A
AddSub1
SineCosine3
Ref V A
Phase Shif B
AddSub
SineCosine4
ReV B
omega*delta_T
Two_PI
Relational
Accumulator
CMult
Phase Shift C
AddSub2
SineCosine5
Ref V C
Current Phase Shift
AddSub3
AddSub6
SineCosine1
Current Gain A
Ref I A
Phase Shift_A
AddSub4
SineCosine6
Current Gain B
Ref I B
Phase Shift_B
AddSub5
SineCosine7
Current Gain C
Ref I C
Phase Shift_C
Ready
109%
ode45

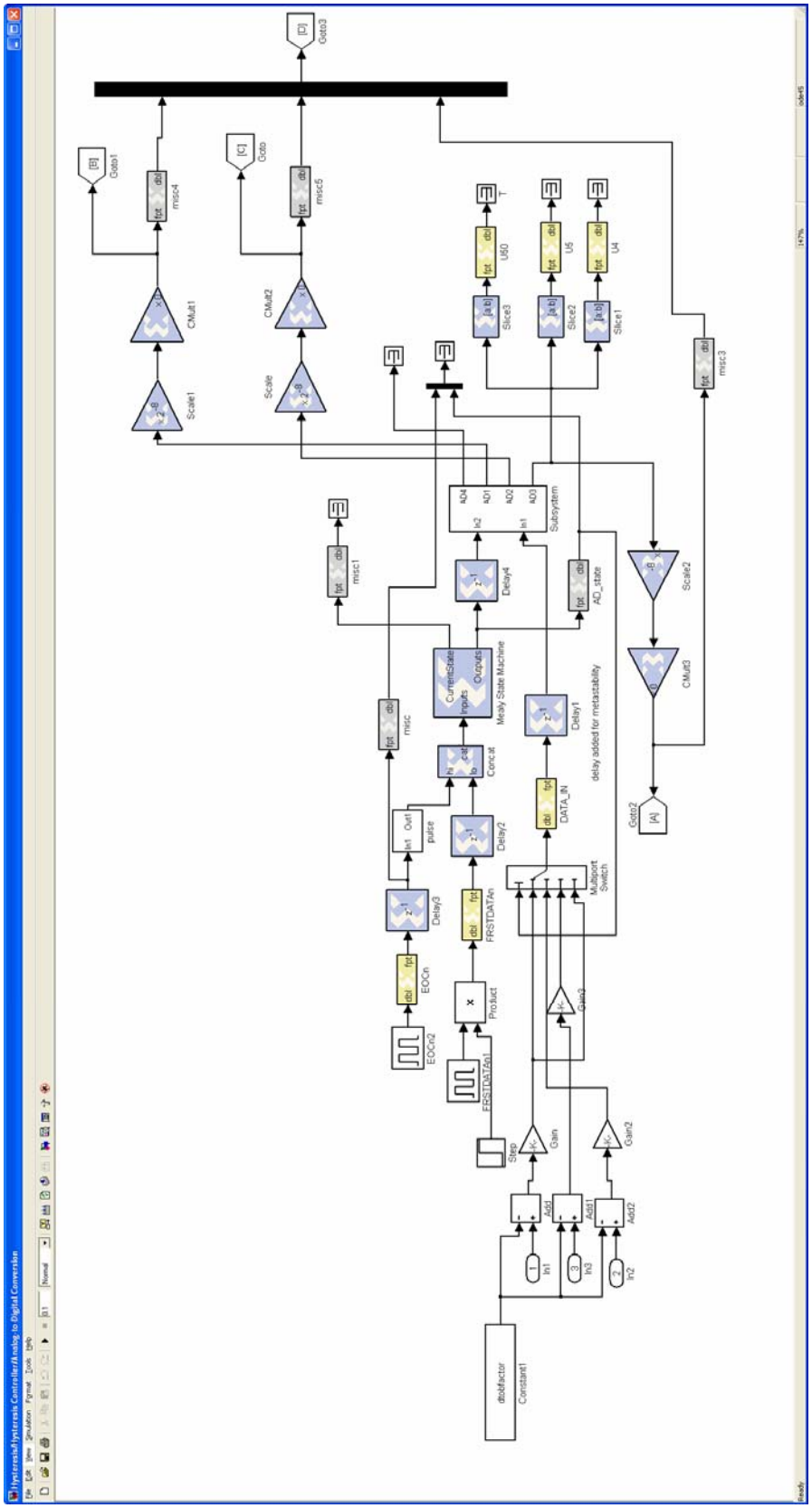

Hysteresis/Bulk Logic
File Edit View Simulation Format Tools Help
Normal
1
Ref A in
sgn
Threshold
[a:b]
Slice
not
Inverter
fpt dbl
U38
1
Qa
fpt dbl
U39
2
Qa1
2
Ref B in
sgn
Threshold1
[a:b]
Slice1
not
Inverter1
fpt dbl
U40
3
Qa2
fpt dbl
U41
4
Qa3
Bulk
Signal
Mux
3
Ref C in
sgn
Threshold2
[a:b]
Slice2
not
Inverter2
fpt dbl
U51
5
Qa4
fpt dbl
U43
6
Qa5
Ready
135%
ode45

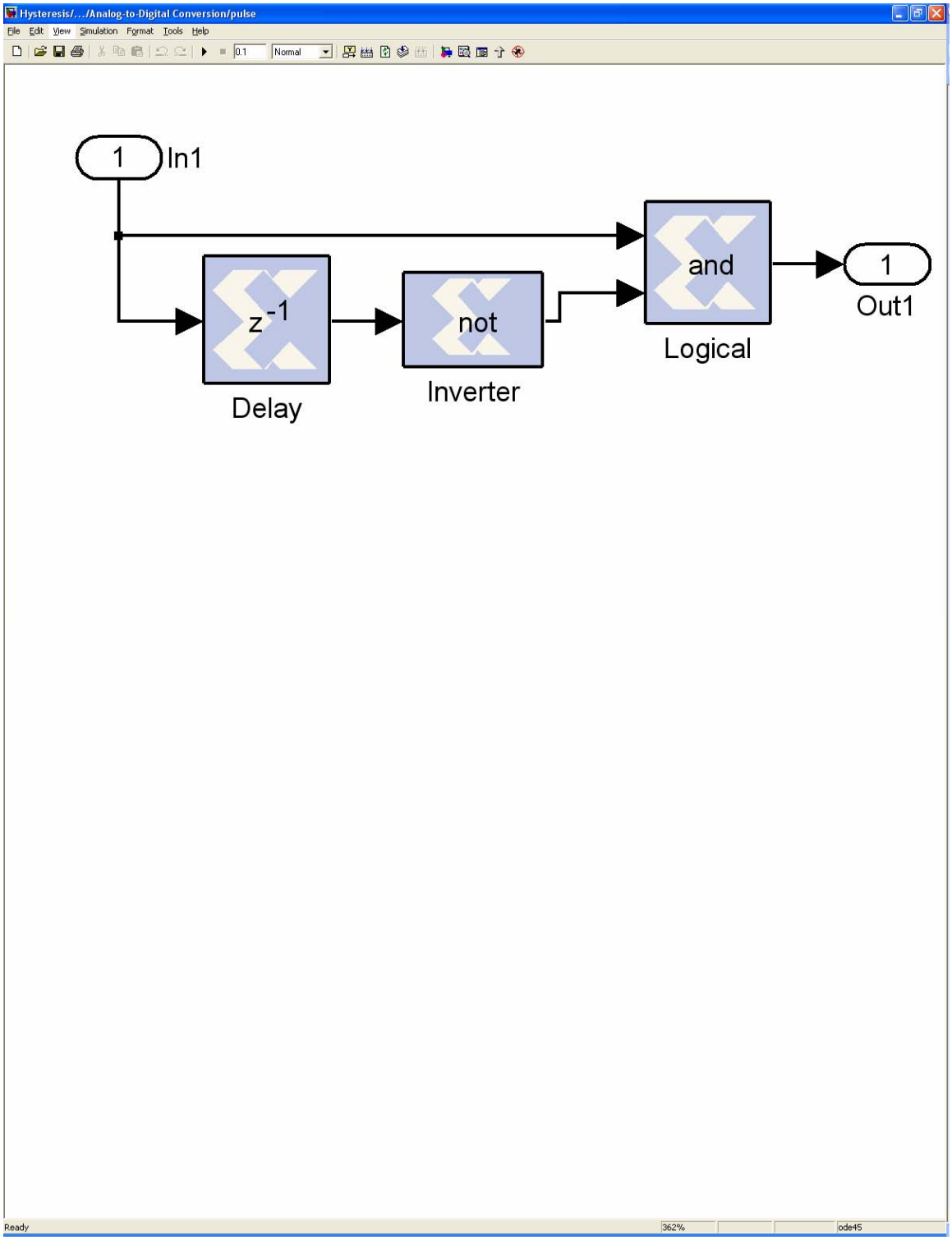

Hysteresis/Hysteresis Controller
File Edit View Simulation Format Tools Help
0.1
Normal
1
I_ref A
2
I_ref B
3
I_ref C
fpt
dbl
U8
U9
U7
Scope3
From3
[D]
In1
In2
In3
Qa
not_Qa
Qb
not_Qb
Qc
not_Qc
1
Qa
2
not_Qa
3
Qb
4
not_Qb
5
Qc
6
not_Qc
Hystersis Control Logic
I_o
I_o
I_o
4
I_n ABC
Bulk
In1
In2
In3
Analog-to-Digital Conversion
Ready
130%
ode45

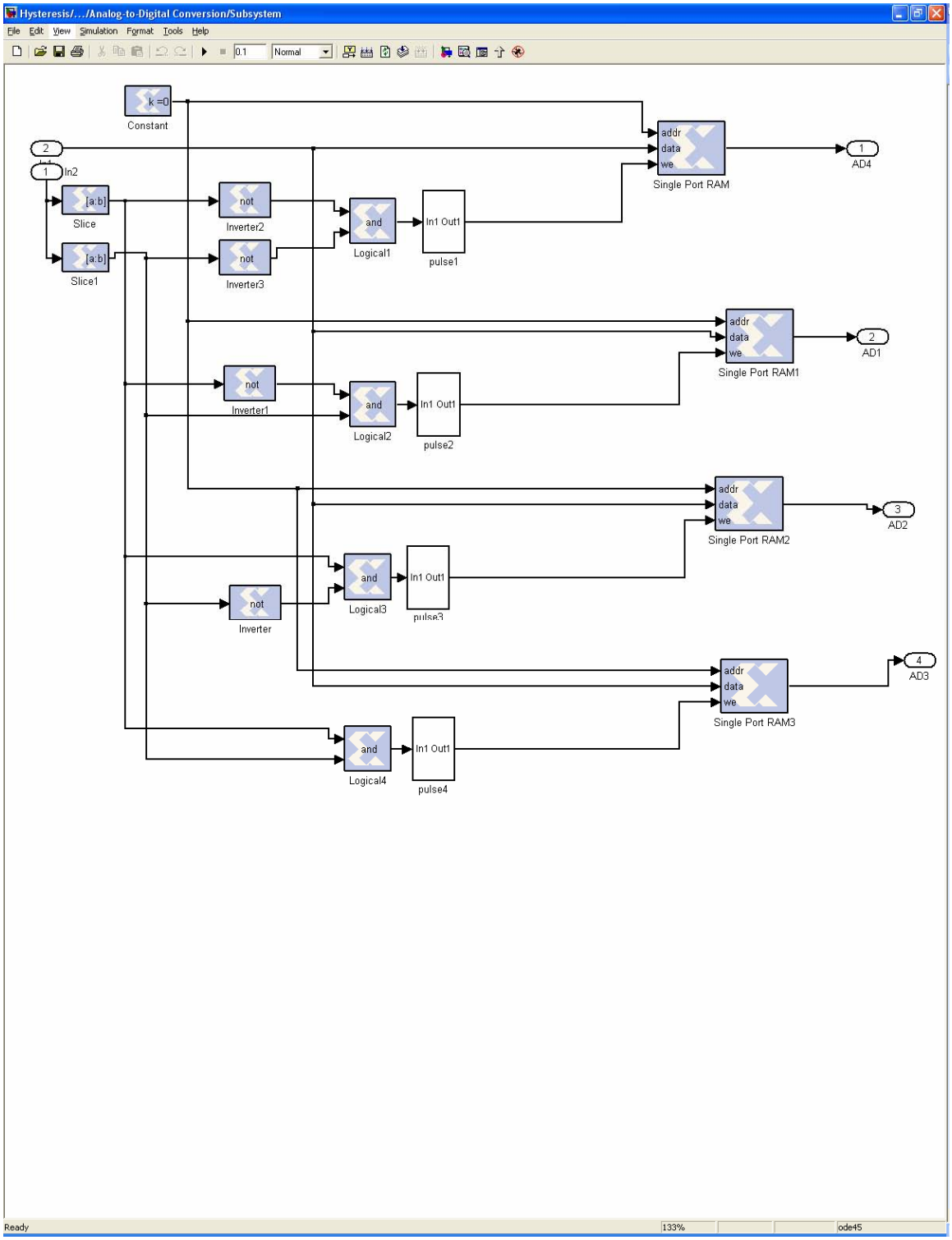

Hysteresis/Hysteresis Controller/Hystersis Control Logic
File Edit View Simulation Format Tools Help
Normal
In1
[A]
From
Constant
k =0
Iref
Iout
delta
So
Ro
Cin
S
NS
Sop
Rop
Co
xSRflipflop1a
MCode
Counter A
out
rst
Register RA
Register SA
Convert
Convert1
cast
fpt
dbl
U 44
U 45
Qa
not_Qa
In2
[B]
From1
MCode1
Counter B
Register RB
Register SB
Convert2
Convert3
U 46
U 47
Qb
not_Qb
In3
[C]
From2
MCode2
Counter C
Register RC
Register SC
Convert4
Convert5
U 48
U 49
Qc
not_Qc
Ready
135%
ode45

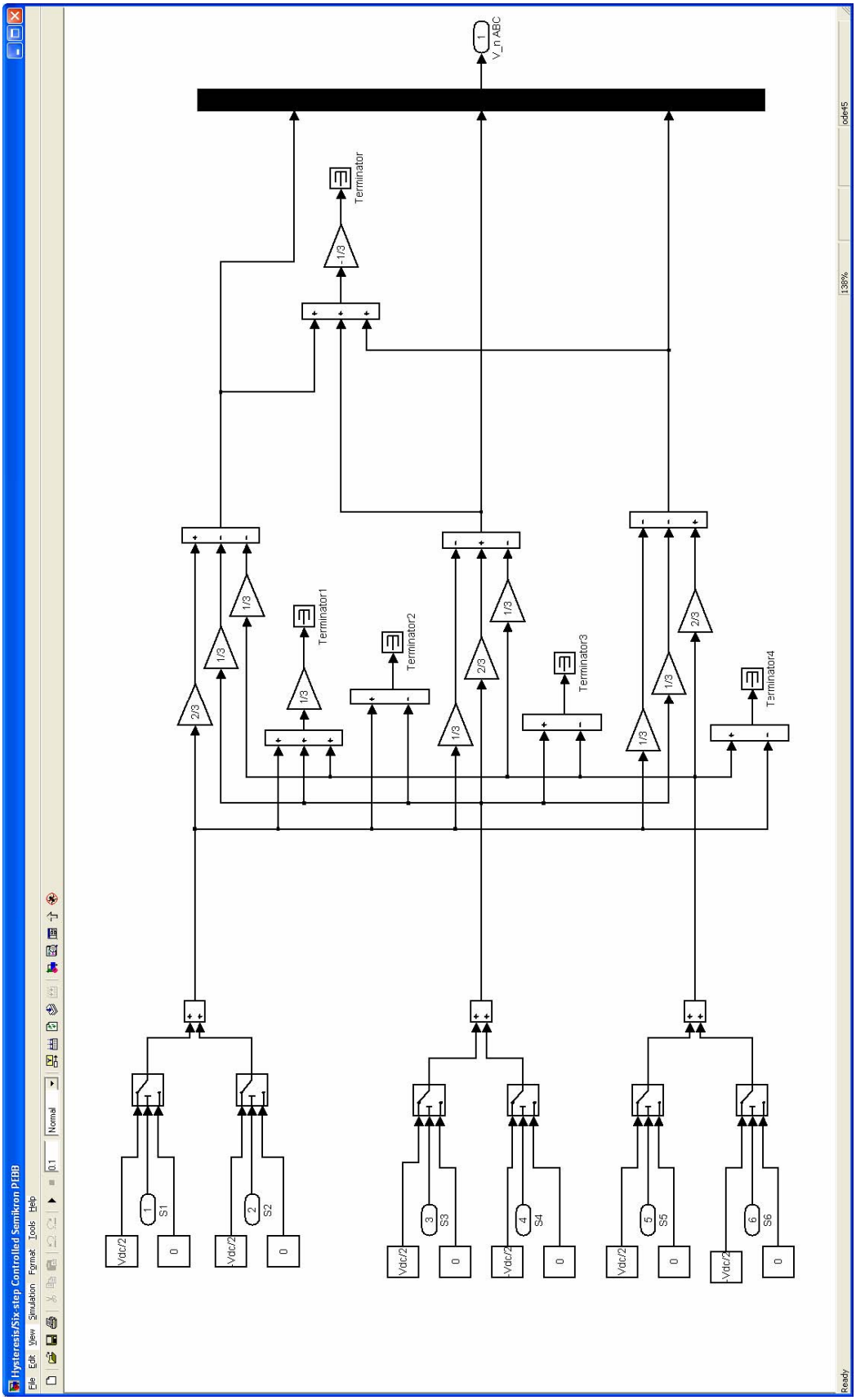
XSRflipflip1a.m

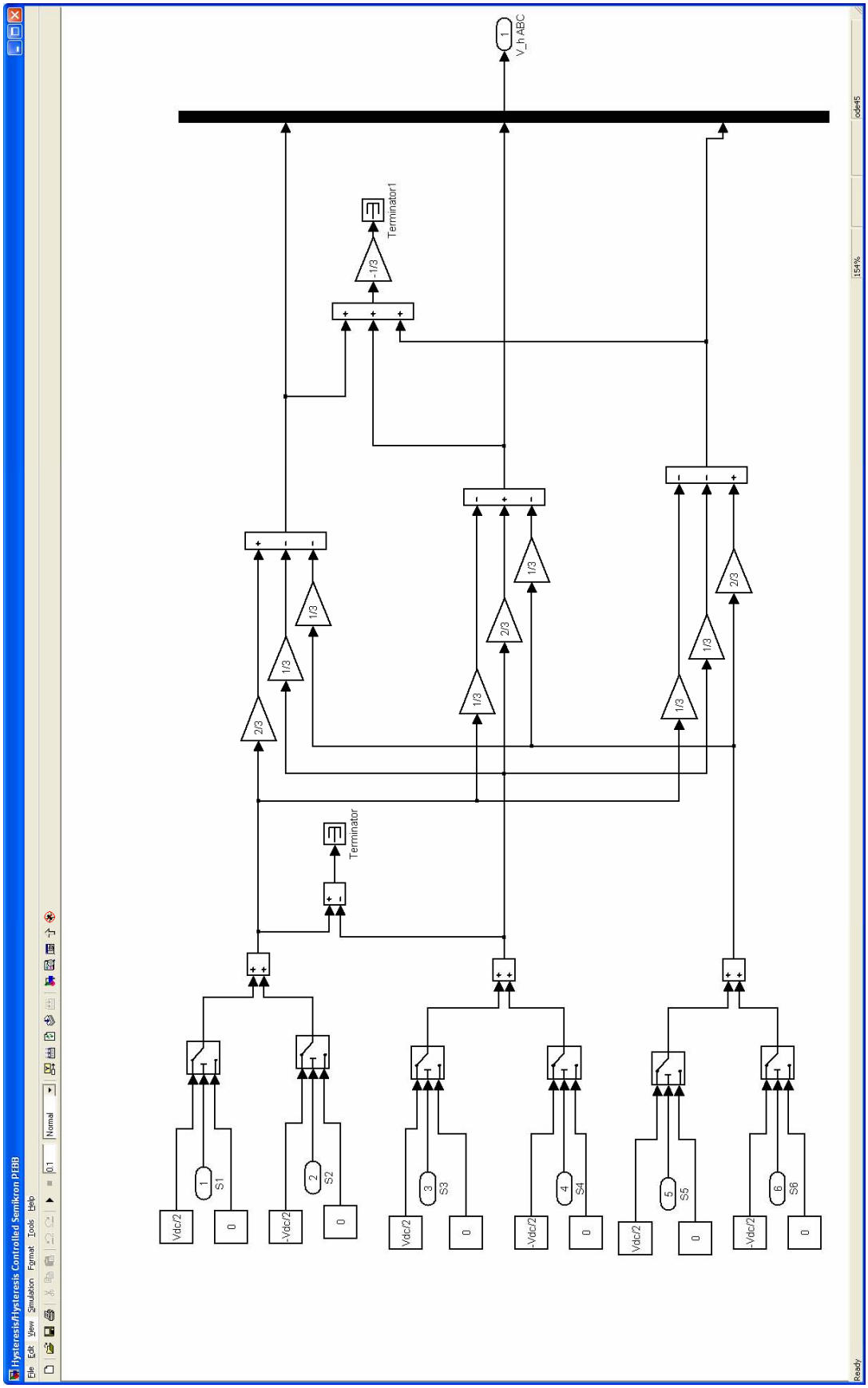
```
function [S ,NS,Sop,Rop,Co] = xSRflipflop(Iref,Iout,delta,So,Ro,Cin)
Sin=0;
Rin=0;
Co = 1==0
const1 = xfix({xlUnsigned, 14, 0}, 1200);
% Co and Cin are used to slow down the switching speed to within the
% allowed limites of the PEEB.  tstep*1200=20k

if ((Iout > Iref + delta/2) & (Iout > 0) & (Cin>1200))
   Rin = 1;
   Co = 1==1;
end
if ((Iout > Iref + delta*2) & (Iout < 0) & (Cin>1200))
   Rin = 1;
   Co = 1==1;
end
if ((Iout < Iref - delta/2) & (Iout < 0) & (Cin>1200))
   Sin = 1;
   Co = 1==1;
end
if ((Iout < Iref - delta*2) & (Iout > 0) & (Cin>1200))
   Sin = 1;
   Co = 1==1;
end


 if Sin == 1
   S=1;
   NS=0;
   Sop=1;
   Rop=0;
 elseif Rin == 1
   S=0;
   NS=1;
   Sop=0;
   Rop=1;
 else
   S=So;
   NS=Ro;
   Sop=So;
   Rop=Ro;
 end
```

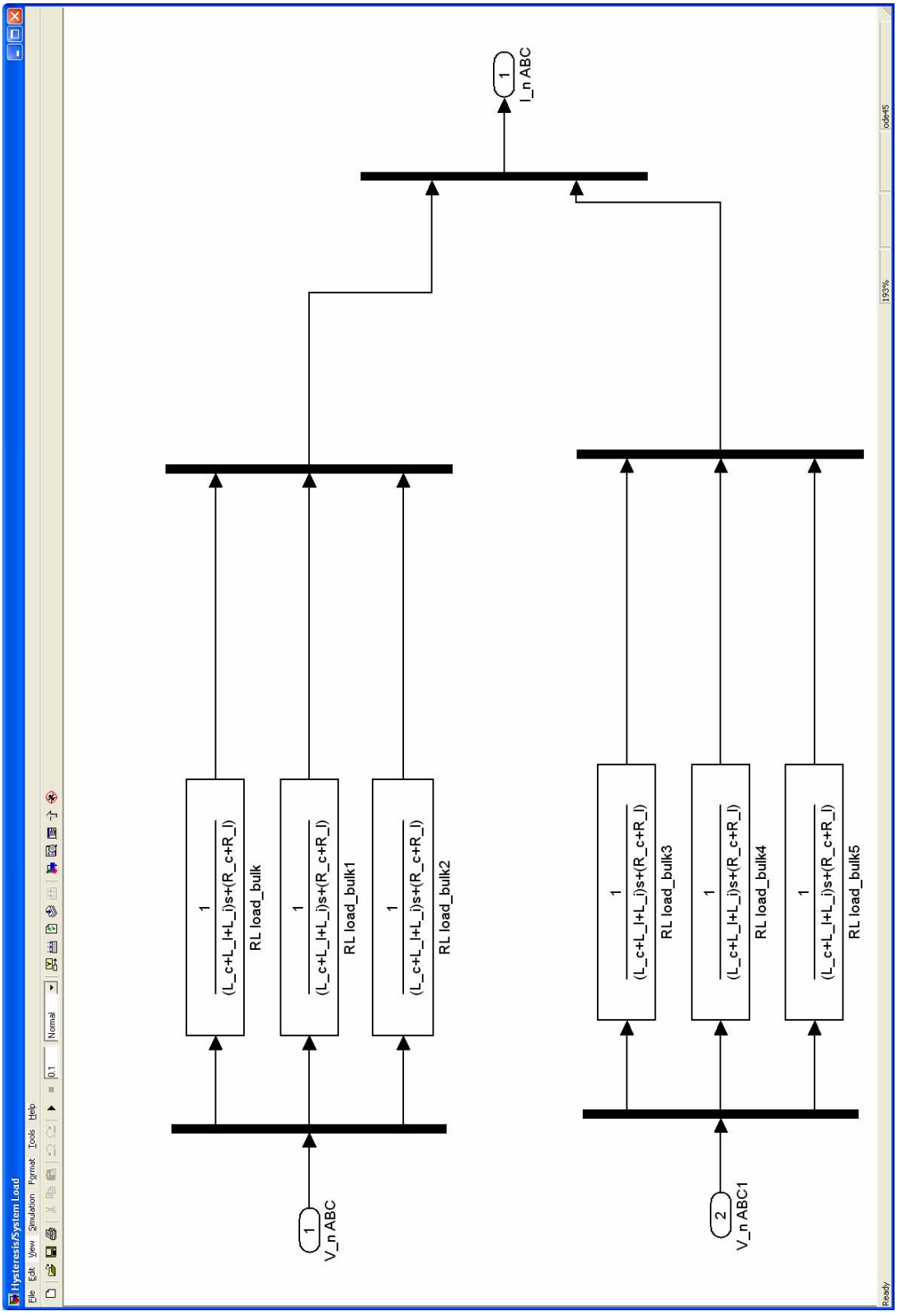

HysteresisAHysteresis Controller(Analog to Digital Converter
Goto3
[B]
Goto1
[C]
Goto
misc4
misc5
CMult1
CMult2
Scale1
Scale
T
U60
U5
U4
Slice3
Slice2
Slice1
misc3
misc1
Subsystem
Delay4
AD_state
Scale2
CMult3
misc
CurrentState
Inputs
Outputs
Mealy State Machine
Concat
Delay1
delay added for metastability
Goto2
[A]
Out1
pulse
Delay2
DATA_IN
Multiport Switch
Delay3
FRSTDATAin
EOCin
EOCin2
Product
FRSTDATAin1
Gain3
Step
Gain
Gain2
Add
Add1
Add2
In1
In3
In2
dtolfactor
Constant1

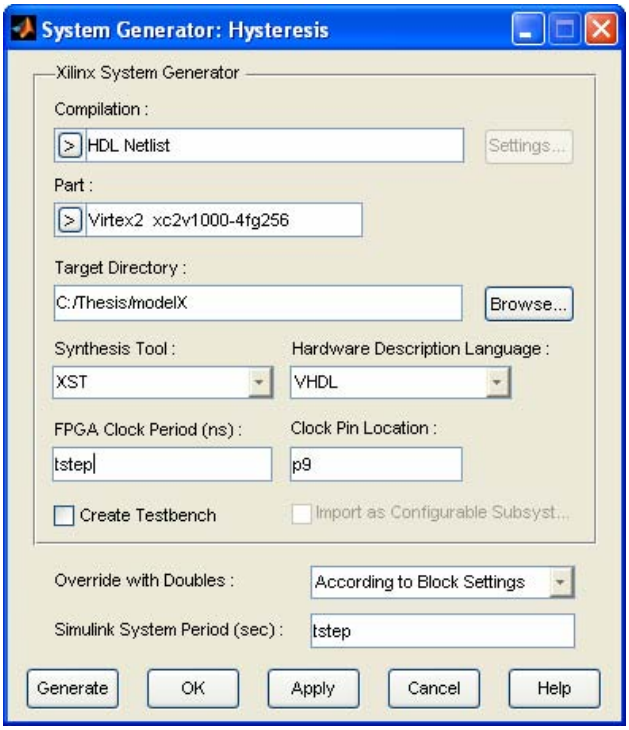

Hysteresis/.../Analog-to-Digital Conversion/pulse
File Edit View Simulation Format Tools Help
Normal
1
In1
z -1
Delay
not
Inverter
and
Logical
1
Out1
Ready
362%
ode45

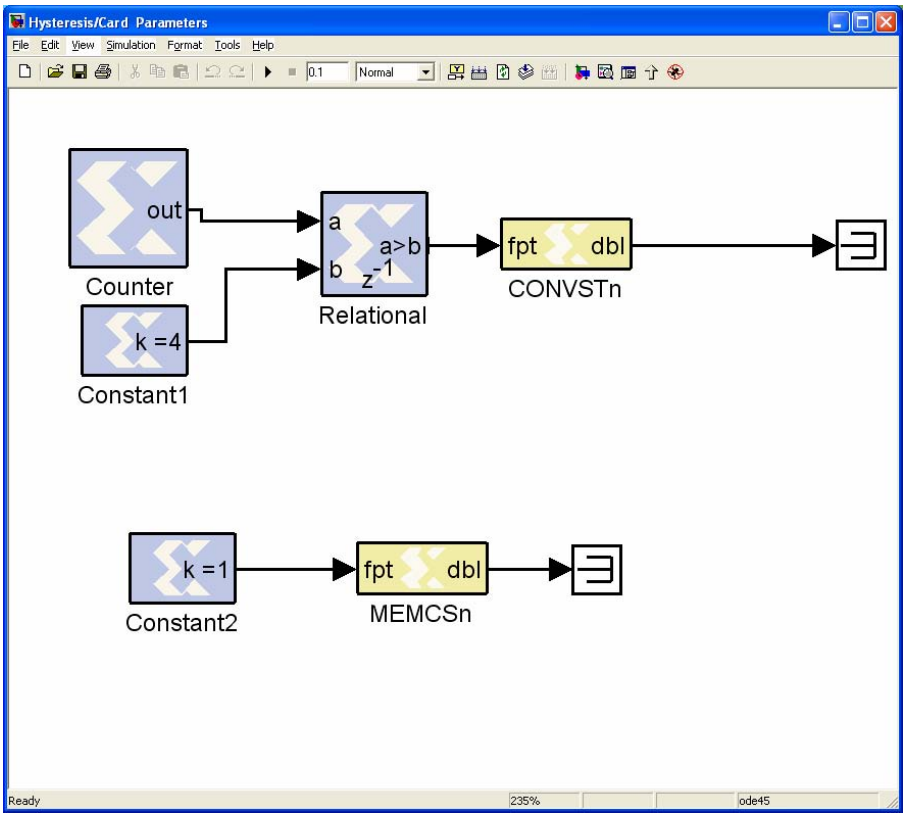

Hysteresis/.../Analog-to-Digital Conversion/Subsystem
File Edit View Simulation Format Tools Help
0.1
Normal
k =0
Constant
2
1
In2
[a:b]
Slice
[a:b]
Slice1
not
Inverter2
not
Inverter3
and
Logical1
In1 Out1
pulse1
addr
data
we
Single Port RAM
1
AD4
addr
data
we
Single Port RAM1
2
AD1
not
Inverter1
and
Logical2
In1 Out1
pulse2
addr
data
we
Single Port RAM2
3
AD2
and
Logical3
In1 Out1
pulse3
not
Inverter
addr
data
we
Single Port RAM3
4
AD3
and
Logical4
In1 Out1
pulse4
Ready
133%
ode45


Hysteresis/Six-step Controlled Semikron PEBB
File Edit View Simulation Format Tools Help
Normal
ode45
138%
Ready
V_n ABC
Terminator
Terminator1
Terminator2
Terminator3
Terminator4
1/3
2/3
Vdc/2
-Vdc/2
S1
S2
S3
S4
S5
S6
0


Hysteresis/Hysteresis Controlled Semikron PEBB
File Edit View Simulation Format Tools Help
Normal
V_h ABC
Terminator1
Terminator
1/3
2/3
Vdc/2
-Vdc/2
0
S1
S2
S3
S4
S5
S6
ode45
154%
Ready


hysteresis/System Load
File Edit View Simulation Format Tools Help
Normal
Ready
100%
ode45
1
V_n ABC
1
(L_c+L_l+L_i)s+(R_c+R_l)
RL load_bulk
1
(L_c+L_l+L_i)s+(R_c+R_l)
RL load_bulk1
1
(L_c+L_l+L_i)s+(R_c+R_l)
RL load_bulk2
1
I_n ABC
2
V_n ABC1
1
(L_c+L_l+L_i)s+(R_c+R_l)
RL load_bulk3
1
(L_c+L_l+L_i)s+(R_c+R_l)
RL load_bulk4
1
(L_c+L_l+L_i)s+(R_c+R_l)
RL load_bulk5


System Generator: Hysteresis
Xilinx System Generator
Compilation :
HDL Netlist
Settings...
Part :
Virtex2 xc2v1000-4fg256
Target Directory :
C:/Thesis/modelX
Browse...
Synthesis Tool :
XST
Hardware Description Language :
VHDL
FPGA Clock Period (ns) :
tstep
Clock Pin Location :
p9
Create Testbench
Import as Configurable Subsyst...
Override with Doubles :
According to Block Settings
Simulink System Period (sec) :
tstep
Generate
OK
Apply
Cancel
Help


Hysteresis/Card Parameters
File Edit View Simulation Format Tools Help
out
Counter
a
b
a>b
z-1
Relational
fpt
dbl
CONVSTn
k =4
Constant1
k =1
Constant2
fpt
dbl
MEMCSn
Ready
235%
ode45

C. M-FILES USED FOR CALCULATIONS AND PICTURE GENERATION

```
% Models FFT/THD calcs

% load saved worksapce 5/19/2006 after running Hysteresis SIMULINK® model

% six-step bulk
load 'C:\Thesis\modelX\workspace5_20_2006_a'
figure(10)
clf
sstart=round(length(BulkCurrent.time)/6)
sstop=round(length(BulkCurrent.time))
plot(BulkCurrent.time(sstart:sstop),BulkCurrent.signals.values(sstart:sstop,3),'b')
hold on
plot(BulkCurrent.time(sstart:sstop),BulkCurrent.signals.values(sstart:sstop,2),'r')
plot(BulkCurrent.time(sstart:sstop),BulkCurrent.signals.values(sstart:sstop,1),'g')
axis([0.005 0.03 -3 3])
grid on
title('Six-Step Three-Phase Line-to-Neutral Current')
xlabel('time')

% figure(11)

figure(12)
plot(TotalwithReference.time,TotalwithReference.signals.values(:,1),'b') %phase a
hold on
plot(TotalwithReference.time,TotalwithReference.signals.values(:,2),'r') %phase b
plot(TotalwithReference.time,TotalwithReference.signals.values(:,3),'g') %phase c
plot(TotalwithReference.time,TotalwithReference.signals.values(:,4),'c') %phase b
plot(TotalwithReference.time,TotalwithReference.signals.values(:,5),'m') %phase c
plot(TotalwithReference.time,TotalwithReference.signals.values(:,6),'y') %phase a
Fs=1/(-TotalwithReference.time(10)+TotalwithReference.time(11))
t=BulkCurrent.time(sstart:sstop);
x=BulkCurrent.signals.values(sstart:sstop,3);
% find one period
nstart = 90000;
nstop = 0;
nflag = 0;
for kk=nstart:sstop
   if(nflag==0 && BulkCurrent.signals.values(kk,3)>=0)
      nstart=kk;
   else
      nflag=1;
   end
    if(nflag==1 && BulkCurrent.signals.values(kk,3)>=0)
       nstop=kk;
    end
end
nstart
nstop

t=BulkCurrent.time(nstart:nstop);
x=BulkCurrent.signals.values(nstart:nstop,3);
```

```
Fs=1/(t(2)-t(1))
Ns=round(Fs/60)
figure(4)
clf
subplot(3,1,1)
plot(t,x,'b');
grid on
subplot(3,1,2)
Pn=abs(fft(x,Ns))*2/length(x);
f=Fs*[0:Ns-1]/Ns;
stem(((1:21)-1)/10,Pn(1:1:21))
subplot(3,1,3)
plot(((1:1:21)-1)/1,20*log10(Pn(1:1:21)/Pn(2)),'*')
stem(((1:1:21)-1)/1,20*log10(Pn(1:1:21)/Pn(2))+60)
set(gca,'YTickLabel',[-60;-50;-40;-30;-20;-10;0])
t_2=length(Pn)/2
Irms=sqrt(sum(Pn(2:1:21).^2))/sqrt(2)
Irms1=Pn(2)/sqrt(2)
Irmsh=sqrt(Irms^2-Irms1^2)
THD=100*Irmsh/Irms1
THDmyway=100*sqrt(sum(Pn(3:21).^2))/Pn(2)

figure(13)
clf
for kk=sstart:sstop
   if(nflag==0 && BulkCurrent.signals.values(kk,1)>=0)
      nstart=kk;
   else
      nflag=1;
   end
    if(nflag==1 && BulkCurrent.signals.values(kk,1)>=0)
       nstop=kk;
    end
end
plot(BulkCurrent.time(nstart:nstop),BulkCurrent.signals.values(nstart:nstop,1),'g')

hold on

plot(TotalwithReference.time(nstart:nstop),TotalwithReference.signals.values(nstart:nstop,1),'b')
%phase a
plot(TotalwithReference.time(nstart:nstop),TotalwithReference.signals.values(nstart:nstop,6),'y')
%phase a


figure(14)
clf
plot(TotalwithReference.time(nstart:nstop),TotalwithReference.signals.values(nstart:nstop,6)-
BulkCurrent.signals.values(nstart:nstop,1),'r') %phase a


figure(14)
clf

Fs=1/(-BulkCurrent.time(11)+BulkCurrent.time(12))
```

```
x=BulkCurrent.signals.values(sstart:sstop,3);
Ns=round(Fs/3)
Pn1=abs(fft(x,Ns))*2/length(x);
f=Fs*[0:Ns-1]/Ns;
Pn1(1)=0;
set(gca,'XTickLabel',[0;2;4;6;8;10;12;14;16;18;20])
set(gca,'YTickLabel',[-60;-50;-40;-30;-20;-10;0])
title('Phase-A Line-to-Neutral');
xlabel('Harmonic')
ylabel('dB')
axis([0 21 1 60])
set(gca,'YTickLabel',[-55;-50;-45;-40;-35;-30;-25;-20;-15;-10;-5;0])
t_2=length(Pn)/2
t_2=21;
Irms=sqrt(sum(Pn1(20:10:201).^2))/sqrt(2)
Irms1=Pn1(10)/sqrt(2)
Irmsh=sqrt(Irms^2-Irms1^2)
THD=100*Irmsh/Irms1
THDmyway=100*sqrt(sum(Pn(3:t_2).^2))/Pn(2)

figure(15)
clf
Fs=1/(-TotalwithReference.time(11)+TotalwithReference.time(12))
Ns=round(Fs/20)
sstart=round(length(TotalwithReference.time)/6)
sstop=round(length(TotalwithReference.time)-1)
x=TotalwithReference.signals.values(sstart:sstop-2,5);      %phase c
Pnh=abs(fft(x,Ns))*2/length(x);
f=Fs*[0:Ns-1]/Ns;
Pnh(1)=0;
stem(((0:3:61)/03),20*log10(Pnh(01:03:062)/Pnh(04))+70,'b')
title('Phase-A Line-to-Neutral');
xlabel('Harmonic')
ylabel('dB')
axis([0 21 1 71])
set(gca,'YTickLabel',[-60;-50;-40;-30;;-20;;-10;;0])
set(gca,'XTickLabel',[0;2;4;6;8;10;12;14;16;18;20])
set(gca,'YTickLabel',[-60;-50;-40;-30;-20;-10;0])
t_2=62;
Irms=sqrt(sum(Pnh(4:3:t_2).^2))/sqrt(2)
Irms1=Pnh(4)/sqrt(2)
Irmsh=sqrt(Irms^2-Irms1^2)
THD=100*Irmsh/Irms1
THDmyway=100*sqrt(sum(Pnh(16:3:t_2).^2))/Pnh(4)
THDmyway=100*sqrt(sum(Pnh(100).^2))/Pnh(20)

 % Examples chapter 2
% Square Wave THD

w=60;
f=2*pi*w;
Fs=1000;
Ts=1/Fs;
t2=-4*pi:0.01:4*pi;
figure(1)
```

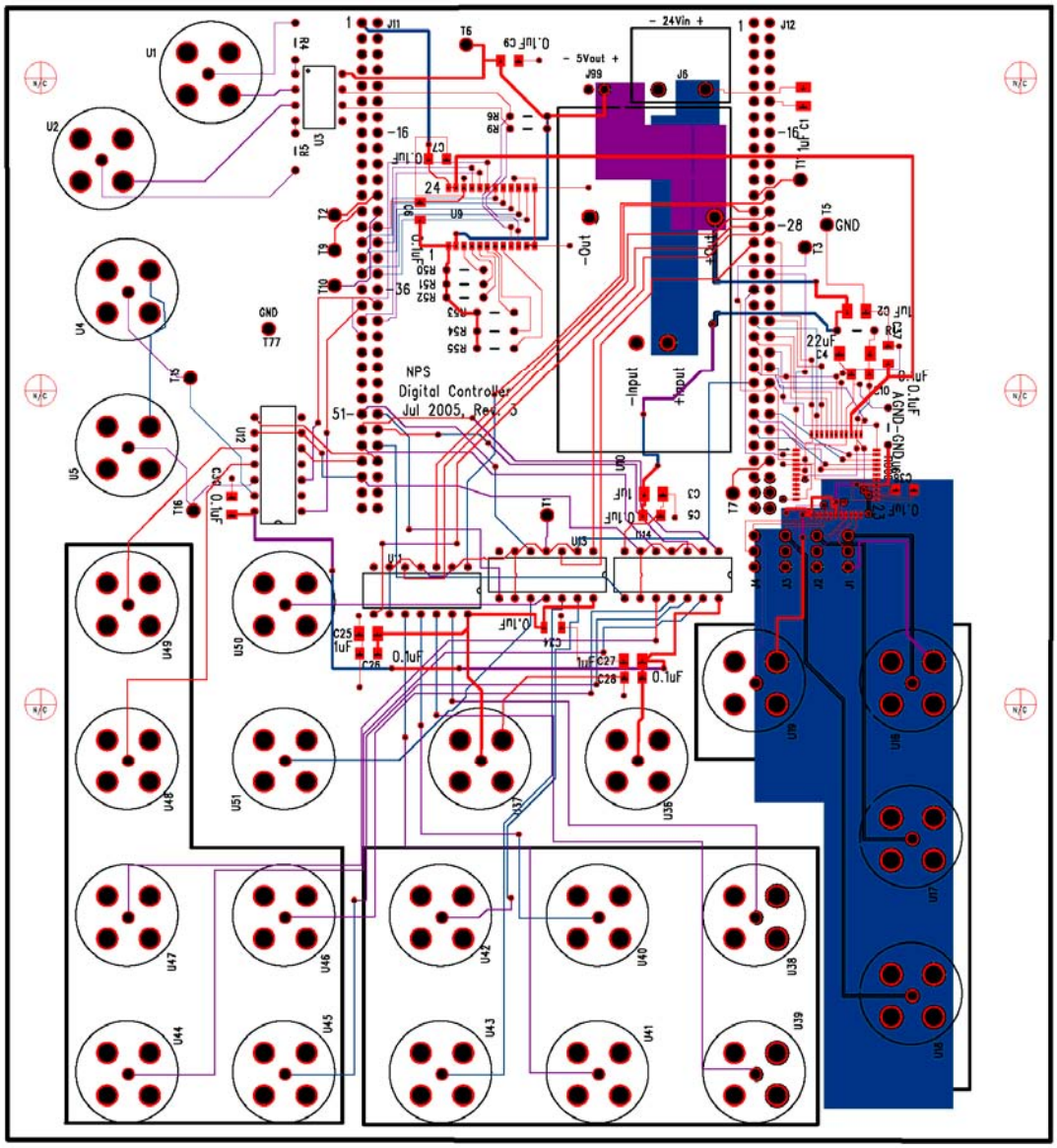
```
subplot(1,2,1)
y2=sign(cos(t2));
plot(t2,y2)
hold on
plot(t2,0,'k')
title('sq(\omegat) f=60Hz')
axis([-13 13 -1.2 1.2])
plot(0,-1.2:0.01:1.2,'k')
t=0:Ts:2*pi;
x=sign(cos(t));
subplot(1,2,2)
Pn=abs(fft(x))*2/length(x);
n=50
stem(0:n-1,Pn(1:n))
title('Fourier Series expansion of sq(\omegat)')
axis([0 50 0 1.4])

t_2=length(Pn)/2
Irms=sqrt(sum(Pn(2:t_2).^2))/sqrt(2)
Irms1=Pn(2)/sqrt(2)
Irmsh=sqrt(Irms^2-Irms1^2)
THD=100*Irmsh/Irms1
THDmyway=100*sqrt(sum(Pn(3:t_2).^2))/Pn(2)
THDactual=100*sqrt((1-(2*sqrt(2)/pi)^2)/(2*sqrt(2)/pi)^2)

% Six step line - to - neutral
w=60;
f=2*pi*w;
Fs=1000;
Ts=1/Fs;
t2=-4*pi:0.001:4*pi;
figure(2)
subplot(1,2,1)
y2=sin(t2);
y3=sin(t2);
for k=1:length(t2)
    y3(k)=sixstep(t2(k));
end
plot(t2,y3)
hold on
plot(t2,0,'k')
title('Van(\theta)')
axis([-13 13 -0.7 0.7])
plot(0,-1.2:0.01:1.2,'k')
t=0:Ts:2*pi;
for k=1:length(t)
    x(k)=sixstep(t(k));
end
subplot(1,2,2)
Pn=abs(fft(x))*2/length(x);
n=50
stem(0:n-1,Pn(1:n))
title('Fourier Series expansion of Van(\theta)')
axis([0 50 0 0.7])
```

```
figure(3)
clf
plot(t2,y3)
hold on
plot(t2,0,'k')
axis([-13 13 -1.2 1.2])
plot(0,-1.2:0.01:1.2,'k')
plot(t2,Pn(2)*sin(t2),'r')
plot(t2,Pn(2)*sin(t2)+Pn(6)*sin(5*t2)+Pn(8)*sin(7*t2),'g')
plot(t2,Pn(2)*sin(t2)+Pn(6)*sin(5*t2)+Pn(8)*sin(7*t2)+ ...
    Pn(12)*sin(11*t2)+Pn(14)*sin(13*t2),'c')
plot(t2,Pn(2)*sin(t2)+Pn(6)*sin(5*t2)+Pn(8)*sin(7*t2)+ ...
    Pn(12)*sin(11*t2)+Pn(14)*sin(13*t2)+ ...
    Pn(18)*sin(17*t2)+Pn(20)*sin(19*t2),'y')

t_2=length(Pn)/2
Irms=sqrt(sum(Pn(2:t_2).^2))/sqrt(2)
Irms1=Pn(2)/sqrt(2)
Irmsh=sqrt(Irms^2-Irms1^2)
THD=100*Irmsh/Irms1
THDmyway=100*sqrt(sum(Pn(3:t_2).^2))/Pn(2)
THDactual=100*sqrt((4/9-(sqrt(2)/(3*pi))^2)/(sqrt(2)/(3*pi))^2)

% Fourier Series
for n=1:17
n
An=(-sin(n*pi/3)+sin(n*2*pi/3)+sin(n*4*pi/3)-sin(n*5*pi/3))/(n*3*pi)
Bn=(-cos(n*pi/3)+cos(n*2*pi/3)+cos(n*4*pi/3)-cos(n*5*pi/3)-2+2*cos(n*pi))/(n*3*pi)
end

THD = sqrt((2/9-(sqrt(2)/(3*pi))^2)/((sqrt(2)/(3*pi))^2))

% Three phase with 4% band
t=0:0.01:2*pi;
y1=sin(t);
y2=sin(t+2*pi/3);
y3=sin(t-2*pi/3);
figure(4)
clf
plot(t,y1,t,y2,t,y3)
hold on
axis([ 0     6.2    -1.3     1.3])
plot(t,y1+0.04,'k',t,y1-0.04,'k')
plot(t,y2+0.04,'k',t,y2-0.04,'k')
plot(t,y3+0.04,'k',t,y3-0.04,'k')
title('Hysteresis Band set to 4%');
xlabel('time')
ylabel('Amplitude')

figure(6)
clf
t=0:0.001:2*pi;
y1=sin(t);
yh=sin(t)+0.04*sawtooth(100*t,0.5);
plot(t,y1,'r',t,y1+0.04,'k',t,y1-0.04,'k',t,yh)
```

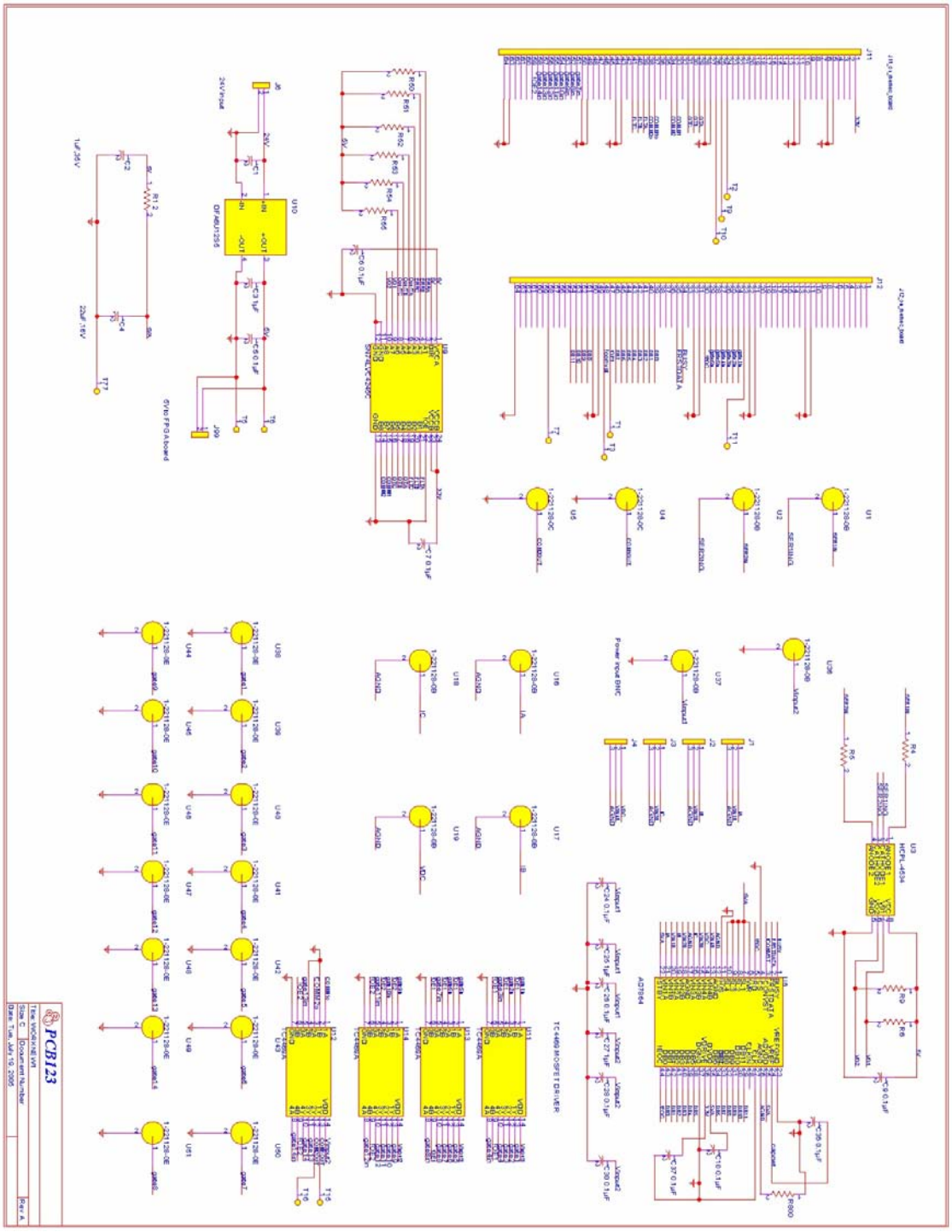
```
hold on
axis([ 0     6.2    -1.3     1.3]);
title('Hysteresis Wave Forms')
xlabel('time');
ylabel('Amplitude')
```

APPENDIX B. NPS CONTROLLER CARD

A. LAYOUT



B. SCHEMATIC



C. NETLIST

PCB123® V2 Netlist for Design fpga_new11.123
Generated on 05/21/06

```
{ Comp 'C1  ' 'CAP1UF     ' '1UFCAP     ' '3.69in' '2.44in' '270.000º' 'Top' }
{ Comp 'C2  ' 'CAP1UF     ' '1UFCAP     ' '3.97in' '1.01in' '0.000º' 'Top' }
{ Comp 'C3  ' 'CAP1UF     ' '1UFCAP     ' '2.675in' '-0.16in' '0.000º' 'Top' }
{ Comp 'C4  ' 'CAP22UF    ' '22UFCAP    ' '3.92in' '0.745in' '0.000º' 'Top' }
{ Comp 'C5  ' 'CAP0P1UF   ' '0.1UFCAP   ' '2.665in' '-0.295in' '0.000º' 'Top' }
{ Comp 'C6  ' 'CAP0P1UF   ' '0.1UFCAP   ' '1.245in' '1.595in' '90.000º' 'Top' }
{ Comp 'C7  ' 'CAP0P1UF   ' '0.1UFCAP   ' '1.3in' '1.9825in' '0.000º' 'Top' }
{ Comp 'C9  ' 'CAP0P1UF   ' '0.1UFCAP   ' '1.76in' '2.61in' '0.000º' 'Top' }
{ Comp 'C10 ' 'CAP0P1UF   ' '0.1UFCAP   ' '4.11in' '0.61in' '180.000º' 'Top' }
{ Comp 'C24 ' ''          ' '0.1UFCAP   ' '2.035in' '-1.01in' '0.000º' 'Top' }
{ Comp 'C25 ' ''          ' '1UFCAP     ' '0.975in' '-1.05in' '180.000º' 'Top' }
{ Comp 'C26 ' ''          ' '0.1UFCAP   ' '0.975in' '-1.175in' '180.000º' 'Top' }
{ Comp 'C27 ' ''          ' '1UFCAP     ' '2.6625in' '-1.225in' '180.000º' 'Top' }
{ Comp 'C28 ' ''          ' '0.1UFCAP   ' '2.6625in' '-1.3275in' '180.000º' 'Top' }
{ Comp 'C30 ' ''          ' '0.1UFCAP   ' '0.045in' '-0.29in' '90.000º' 'Top' }
{ Comp 'C36 ' ''          ' '0.1UFCAP   ' '4.28in' '-0.13in' '0.000º' 'Top' }
{ Comp 'C37 ' ''          ' '0.1UFCAP   ' '4.23in' '0.68in' '90.000º' 'Top' }
{ Comp 'J1  ' 'CONN3A     ' 'JMPR       ' '3.975in' '-0.425in' '0.000º' 'Top' }
{ Comp 'J2  ' 'CONN3A     ' 'JMPR       ' '3.775in' '-0.425in' '0.000º' 'Top' }
{ Comp 'J3  ' 'CONN3A     ' 'JMPR       ' '3.575in' '-0.425in' '0.000º' 'Top' }
{ Comp 'J4  ' 'CONN3A     ' 'JMPR       ' '3.375in' '-0.425in' '0.000º' 'Top' }
{ Comp 'J6  ' 'CONN2A     ' 'POWERCONN  ' '3.065in' '2.425in' '270.000º' 'Top' }
{ Comp 'J11 ' 'CONN64B    ' 'CONN64HOLES' '0.875in' '2.85in' '0.000º' 'Top' }
{ Comp 'J12 ' 'CONN64A    ' 'CONN64HOLES' '3.375in' '2.85in' '0.000º' 'Top' }
{ Comp 'J99 ' 'CONN2A     ' 'JMPR2PIN   ' '2.42in' '2.425in' '270.000º' 'Top' }
{ Comp 'R1  ' 'RESISTORA  ' 'RESEIGHTH  ' '3.905in' '0.89in' '0.000º' 'Top' }
{ Comp 'R4  ' 'RESISTORA  ' 'RESEIGHTH  ' '0.45in' '2.85in' '270.000º' 'Top' }
{ Comp 'R5  ' 'RESISTORA  ' 'RESEIGHTH  ' '0.45in' '1.91in' '90.000º' 'Top' }
{ Comp 'R6  ' 'RESISTORA  ' 'RESEIGHTH  ' '2.055in' '2.255in' '180.000º' 'Top' }
{ Comp 'R9  ' 'RESISTORA  ' 'RESEIGHTH  ' '2.055in' '2.175in' '180.000º' 'Top' }
{ Comp 'R50 ' ''          ' 'RESEIGHTH  ' '1.65in' '1.275in' '180.000º' 'Top' }
{ Comp 'R51 ' ''          ' 'RESEIGHTH  ' '1.65in' '1.185in' '180.000º' 'Top' }
{ Comp 'R52 ' ''          ' 'RESEIGHTH  ' '1.65in' '1.1in' '180.000º' 'Top' }
{ Comp 'R53 ' ''          ' 'RESEIGHTH  ' '1.845in' '1.005in' '180.000º' 'Top' }
{ Comp 'R54 ' ''          ' 'RESEIGHTH  ' '1.845in' '0.885in' '180.000º' 'Top' }
{ Comp 'R55 ' ''          ' 'RESEIGHTH  ' '1.845in' '0.775in' '180.000º' 'Top' }
{ Comp 'R800' '           ' 'RESEIGHTH  ' '4.23in' '0.39in' '270.000º' 'Top' }
{ Comp 'T1  ' 'TESTPOINT  ' 'TESTPT     ' '2.055in' '-0.295in' '0.000º' 'Top' }
{ Comp 'T2  ' 'TESTPOINT  ' 'TESTPT     ' '0.7in' '1.625in' '0.000º' 'Top' }
{ Comp 'T3  ' 'TESTPOINT  ' 'TESTPT     ' '3.7in' '1.42in' '0.000º' 'Top' }
{ Comp 'T5  ' 'TESTPOINT  ' 'TESTPT     ' '3.84in' '1.565in' '0.000º' 'Top' }
{ Comp 'T6  ' 'TESTPOINT  ' 'TESTPT     ' '1.54in' '2.71in' '0.000º' 'Top' }
{ Comp 'T7  ' 'TESTPOINT  ' 'TESTPT     ' '3.24in' '-0.155in' '0.000º' 'Top' }
{ Comp 'T9  ' 'TESTPOINT  ' 'TESTPT     ' '0.7in' '1.4in' '0.000º' 'Top' }
{ Comp 'T10 ' 'TESTPOINT  ' 'TESTPT     ' '0.7in' '1.175in' '0.000º' 'Top' }
```

```
{ Comp 'T11 ' 'TESTPOINT   ' 'TESTPT     ' '3.67in' '1.85in' '0.000º' 'Top' }
{ Comp 'T15 ' 'TESTPOINT   ' 'TESTPT     ' '-0.22in' '0.58in' '0.000º' 'Top' }
{ Comp 'T16 ' 'TESTPOINT   ' 'TESTPT     ' '-0.2in' '-0.265in' '0.000º' 'Top' }
{ Comp 'T77 ' '            ' 'TESTPT     ' '0.28in' '0.9in' '0.000º' 'Top' }
{ Comp 'U1  ' '1-221128-0B ' 'BNCVERT    ' '-0.24in' '2.66in' '270.000º' 'Top' }
{ Comp 'U2  ' '1-221128-0B ' 'BNCVERT    ' '-0.92in' '2.11in' '270.000º' 'Top' }
{ Comp 'U3  ' 'HCPL-4534   ' 'DIP8       ' '0.45in' '2.525in' '0.000º' 'Top' }
{ Comp 'U4  ' '1-221128-0C ' 'BNCVERT    ' '-0.75in' '1in' '0.000º' 'Top' }
{ Comp 'U5  ' '1-221128-0C ' 'BNCVERT    ' '-0.75in' '0in' '0.000º' 'Top' }
{ Comp 'U6  ' 'AD7864      ' 'MQFP44     ' '3.9in' '-0.035in' '270.000º' 'Top' }
{ Comp 'U9  ' 'SN74LVC4245B' 'TSSOP24B   ' '1.425in' '1.43in' '0.000º' 'Top' }
{ Comp 'U10 ' 'DFA6U12S5   ' 'POWERDFA6  ' '2.625in' '0.81in' '90.000º' 'Top' }
{ Comp 'U11 ' 'TC4469A     ' 'DIP14      ' '1.55in' '-0.625in' '270.000º' 'Top' }
{ Comp 'U12 ' 'TC4469A     ' 'DIP14      ' '0.49in' '-0.27in' '180.000º' 'Top' }
{ Comp 'U13 ' 'TC4469A     ' 'DIP14      ' '2.35in' '-0.525in' '270.000º' 'Top' }
{ Comp 'U14 ' 'TC4469A     ' 'DIP14      ' '3.15in' '-0.525in' '270.000º' 'Top' }
{ Comp 'U16 ' '1-221128-0B ' 'BNCVERT    ' '4.25in' '-1.5in' '0.000º' 'Top' }
{ Comp 'U17 ' '1-221128-0B ' 'BNCVERT    ' '4.25in' '-2.5in' '0.000º' 'Top' }
{ Comp 'U18 ' '            ' 'BNCVERT    ' '4.25in' '-3.5in' '0.000º' 'Top' }
{ Comp 'U19 ' '            ' 'BNCVERT    ' '3.25in' '-1.5in' '0.000º' 'Top' }
{ Comp 'U36 ' '            ' 'BNCVERT    ' '2.5in' '-2in' '0.000º' 'Top' }
{ Comp 'U37 ' '            ' 'BNCVERT    ' '1.5in' '-2in' '0.000º' 'Top' }
{ Comp 'U38 ' '            ' 'BNCVERT    ' '3.25in' '-3in' '0.000º' 'Top' }
{ Comp 'U39 ' '            ' 'BNCVERT    ' '3.25in' '-4in' '0.000º' 'Top' }
{ Comp 'U40 ' '            ' 'BNCVERT    ' '2.25in' '-3in' '0.000º' 'Top' }
{ Comp 'U41 ' '            ' 'BNCVERT    ' '2.25in' '-4in' '0.000º' 'Top' }
{ Comp 'U42 ' '            ' 'BNCVERT    ' '1.25in' '-3in' '0.000º' 'Top' }
{ Comp 'U43 ' '            ' 'BNCVERT    ' '1.25in' '-4in' '0.000º' 'Top' }
{ Comp 'U44 ' '            ' 'BNCVERT    ' '-0.75in' '-4in' '0.000º' 'Top' }
{ Comp 'U45 ' '            ' 'BNCVERT    ' '0.25in' '-4in' '0.000º' 'Top' }
{ Comp 'U46 ' '            ' 'BNCVERT    ' '0.25in' '-3in' '0.000º' 'Top' }
{ Comp 'U47 ' '            ' 'BNCVERT    ' '-0.75in' '-3in' '0.000º' 'Top' }
{ Comp 'U48 ' '            ' 'BNCVERT    ' '-0.75in' '-2in' '0.000º' 'Top' }
{ Comp 'U49 ' '            ' 'BNCVERT    ' '-0.75in' '-1in' '0.000º' 'Top' }
{ Comp 'U50 ' '            ' 'BNCVERT    ' '0.25in' '-1in' '0.000º' 'Top' }
{ Comp 'U51 ' '            ' 'BNCVERT    ' '0.25in' '-2in' '0.000º' 'Top' }

{ Net '!CONVST'
'U6.3' 'J12.48' 'T3.1'
}
{ Net '!EOC'
'U6.44' 'J12.30' 'U6.5'
}
{ Net '!OE1'
'J12.47' 'T1.1' 'U11.2' 'U11.4' 'U11.6' 'U11.9' 'U13.2' 'U13.4'
'U13.6' 'U13.9'
}
{ Net '!OE2'
'J11.59' 'U12.6' 'U12.9' 'U14.2' 'U14.4' 'U14.6' 'U14.9'
}
{ Net '3.3V'
```

'U6.36' 'J11.1' 'C7.1' 'C37.1' 'U9.23' 'U9.24'
}
{ Net '5V'
'U3.8' 'T6.1' 'U10.3' 'J99.1' 'C5.1' 'C6.1' 'C9.1' 'C2.1'
'C3.1' 'R1.1' 'R6.1' 'R9.1' 'R50.2' 'R55.2' 'R54.2' 'R53.2'
'R52.2' 'R51.2' 'U9.1' 'U9.2'
}
{ Net '5VA'
'U6.6' 'U6.9' 'U6.7' 'U6.8' 'U6.10' 'U6.25' 'U6.35' 'U6.22'
'C4.1' 'C10.1' 'R1.2'
}
{ Net '24V'
'J6.1' 'U10.1' 'C1.1'
}
{ Net 'AGND'
'U6.17' 'U6.26' 'U6.12' 'R800.2' 'U19.2' 'U18.2' 'U16.2' 'U17.2'
'J1.3' 'J4.3' 'J3.3' 'J2.3'
}
{ Net 'BUSY'
'U6.1' 'J12.34'
}
{ Net 'CAPNET'
'U6.24' 'C36.1'
}
{ Net 'COM1OUT'
'U12.13' 'T15.1' 'U4.1'
}
{ Net 'COM2OUT'
'U12.12' 'T16.1' 'U5.1'
}
{ Net 'COMM1'
'J11.33' 'U9.15'
}
{ Net 'COMM1O'
'J11.37' 'U12.1'
}
{ Net 'COMM2'
'J11.34' 'U9.14'
}
{ Net 'COMM2O'
'J11.38' 'U12.3'
}
{ Net 'DB0'
'U6.43' 'J12.39'
}
{ Net 'DB1'
'U6.42' 'J12.40'
}
{ Net 'DB2'
'U6.41' 'J12.41'
}

{ Net 'DB3'
'U6.40' 'J12.42'
}
{ Net 'DB4'
'U6.39' 'J12.43'
}
{ Net 'DB5'
'U6.38' 'J12.44'
}
{ Net 'DB6'
'U6.34' 'J12.45'
}
{ Net 'DB7'
'U6.33' 'J12.46'
}
{ Net 'DB8'
'U6.32' 'J12.51'
}
{ Net 'DB9'
'U6.31' 'J12.52'
}
{ Net 'DB10'
'U6.30' 'J12.53'
}
{ Net 'DB11'
'U6.29' 'J12.54'
}
{ Net 'DEF0_1'
'U3.1' 'R4.2'
}
{ Net 'DEF1_1'
'U3.4' 'R5.2'
}
{ Net 'DEF2_1'
'J12.23' 'T11.1'
}
{ Net 'DEF3_1'
'J12.58' 'T7.1'
}
{ Net 'DEF4_1'
'J11.24' 'T2.1'
}
{ Net 'DEF5_1'
'J11.25' 'T9.1'
}
{ Net 'DEF6_1'
'J11.26' 'T10.1'
}
{ Net 'ERRA'
'R50.1' 'U9.3'
}

{ Net 'ERRB'
'R51.1' 'U9.4'
}
{ Net 'ERRC'
'R52.1' 'U9.5'
}
{ Net 'FLTA'
'J11.39' 'U9.21'
}
{ Net 'FLTB'
'J11.40' 'U9.20'
}
{ Net 'FLTC'
'J11.41' 'U9.19'
}
{ Net 'FRSTDATA'
'U6.2' 'J12.35'
}
{ Net 'GATE1'
'U11.13' 'U38.1'
}
{ Net 'GATE1IN'
'J12.24' 'U11.1'
}
{ Net 'GATE2'
'U11.12' 'U39.1'
}
{ Net 'GATE2IN'
'J12.25' 'U11.3'
}
{ Net 'GATE3'
'U11.11' 'U40.1'
}
{ Net 'GATE3IN'
'J12.26' 'U11.5'
}
{ Net 'GATE4'
'U11.10' 'U41.1'
}
{ Net 'GATE4IN'
'J12.27' 'U11.8'
}
{ Net 'GATE5'
'U13.13' 'U42.1'
}
{ Net 'GATE5IN'
'J12.28' 'U13.1'
}
{ Net 'GATE6'
'U13.12' 'U43.1'
}

{ Net 'GATE6IN'
'J12.29' 'U13.3'
}
{ Net 'GATE7'
'U13.11' 'U50.1'
}
{ Net 'GATE7IN'
'J11.51' 'U13.5'
}
{ Net 'GATE8'
'U13.10' 'U51.1'
}
{ Net 'GATE8IN'
'J11.52' 'U13.8'
}
{ Net 'GATE9'
'U14.13' 'U44.1'
}
{ Net 'GATE9IN'
'J11.53' 'U14.1'
}
{ Net 'GATE10'
'U14.12' 'U45.1'
}
{ Net 'GATE10IN'
'J11.54' 'U14.3'
}
{ Net 'GATE11'
'U14.11' 'U46.1'
}
{ Net 'GATE11IN'
'J11.55' 'U14.5'
}
{ Net 'GATE12'
'U14.10' 'U47.1'
}
{ Net 'GATE12IN'
'J11.56' 'U14.8'
}
{ Net 'GATE13'
'U12.11' 'U48.1'
}
{ Net 'GATE13IN'
'J11.57' 'U12.5'
}
{ Net 'GATE14'
'U12.10' 'U49.1'
}
{ Net 'GATE14IN'
'J11.58' 'U12.8'
}

{ Net 'GROUND'
'U3.5' 'U6.4' 'U6.11' 'U6.23' 'U6.27' 'U6.37' 'J12.11' 'J12.12'
'J12.21' 'J12.22' 'J12.31' 'J12.32' 'J12.49' 'J12.50' 'J12.64' 'J11.5'
'J11.6' 'J11.11' 'J11.12' 'J11.27' 'J11.28' 'J11.43' 'J11.44' 'J11.49'
'J11.50' 'J11.63' 'J11.64' 'T5.1' 'U11.7' 'U12.2' 'U12.4' 'U12.7'
'U13.7' 'U14.7' 'J6.2' 'C4.2' 'U10.2' 'U10.4' 'J99.2' 'T77.1'
'C5.2' 'C6.2' 'C7.2' 'C9.2' 'C10.2' 'C28.2' 'C26.2' 'C30.2'
'C36.2' 'C37.2' 'C1.2' 'C2.2' 'C3.2' 'C27.2' 'C25.2' 'R800.1'
'U37.2' 'U38.2' 'U39.2' 'U40.2' 'U41.2' 'U42.2' 'U43.2' 'U44.2'
'U45.2' 'U46.2' 'U47.2' 'U48.2' 'U49.2' 'U50.2' 'U51.2' 'U36.2'
'U4.2' 'U5.2' 'U9.11' 'U9.12' 'U9.13' 'U9.22' 'C24.2'
}
{ Net 'IA'
'U6.21' 'J1.1' 'U16.1'
}
{ Net 'IB'
'U6.19' 'J2.1' 'U17.1'
}
{ Net 'IC'
'U6.16' 'J3.1' 'U18.1'
}
{ Net 'OTA'
'J11.29' 'U9.18'
}
{ Net 'OTB'
'J11.30' 'U9.17'
}
{ Net 'OTC'
'J11.31' 'U9.16'
}
{ Net 'OVERTA'
'R53.1' 'U9.6'
}
{ Net 'OVERTB'
'R54.1' 'U9.7'
}
{ Net 'OVERTC'
'R55.1' 'U9.8'
}
{ Net 'SER1IN'
'R4.1' 'U1.1'
}
{ Net 'SER1ING'
'U3.2' 'U1.2'
}
{ Net 'SER2IN'
'R5.1' 'U2.1'
}
{ Net 'SER2ING'
'U3.3' 'U2.2'
}

{ Net 'VDC'
'U6.14' 'J4.1' 'U19.1'
}
{ Net 'VIN1B'
'U6.20' 'J1.2'
}
{ Net 'VIN2B'
'U6.18' 'J2.2'
}
{ Net 'VIN3B'
'U6.15' 'J3.2'
}
{ Net 'VIN4B'
'U6.13' 'J4.2'
}
{ Net 'VINPUT1'
'U11.14' 'U13.14' 'C25.1' 'C26.1' 'U37.1' 'C24.1'
}
{ Net 'VINPUT2'
'C27.1' 'C28.1' 'U12.14' 'U14.14' 'C30.1' 'U36.1'
}
{ Net 'VO1'
'U3.7' 'R6.2' 'U9.9'
}
{ Net 'VO2'
'U3.6' 'R9.2' 'U9.10'
}

D. BOM

Part Description	Manufacturer	Vendor Part #
Vertical BNC	Digikey	A24517-ND
Dual Optocoupler for gate drives	Fairchild	HCPL2531
A/D Converter, 4 channels, 12 bits	Analog devices	AD7864AS-1
CAPACITOR TANT 1.0UF 35V 10% SMD	Kemet	T491B105K035AS
22 μF tantalum caps, 16V rated part	Kemet	T494C226M016AS
0.1 μF ceramic caps, 25V rated part, 1206 pkg	Panasonic	
IC MOSFET DVR AND/INV 14DIP	Microchip	TC4469CPD
IC OCT BUS XCVR/SHIFTER 24-TSSOP	Texas Inst.	SN74LVC4245APWR
TinyLogic UHS Inverter (Open Drain Output)	Fairchild	NC7SZ05M5
IC QUAD 2-INPUT AND GATE 14-SOIC	Texas Inst.	SN74LVC08ADR
IC VOLT REG ADJ MICRPWR TO-92	National	LP2950ACZ-5.0
CONN JACK BNC R/A 50OHM PCB TIN	AMP	227161-1
CONN HEADER FEM 64POS .1" DL TIN	Sullins	PPTC322LFBN
Test points (drill 0.063" hole)	Keystone	5010
PROTECT HEADER RT/ANG 14 CONTACT	3M	3314-5002
TERM BLOCK PLUG 7.62MM 2POS PCB	On Shore	EDZ960/2
TERM BLOCK HDR 7.62MM 2POS PCB	On Shore	EDSTLZ960/2
RES ARRAY 10KOHM 16TERM 8RES SMD	CTS	741X163103J

E. PIN OUT

SIMULINK®	Card	Pin	FPGA
Bulk A	U38	J12-24	C16
Bulk A'	U39	J12-25	D16
Bulk B	U40	J12-26	E13
Bulk B'	U41	J12-27	H13
Bulk C	U42	J12-28	H14
Bulk C'	U43	J12-29	H15
Hyst A	U44	J11-53	L5
Hyst A'	U45	J11-54	T6
Hyst B	U46	J11-55	T5
Hyst B'	U47	J11-56	N6
Hyst C	U48	J11-57	P6
Hyst C'	U49	J11-58	P7
	U50	J11-51	M2
	U51	J11-52	M6
	U 4	J11-37	H3
	U 5	J11-38	H4
EOCn		J12-30	H16
FRSTDATAn		J12-35	L12
I A	U16	I A	
I B	U17	I B	
I C	U18	I C	
	U19	VDC	
CONVSTn		J12-48	J14
MEMCSn			J15

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APPENDIX C. COMMERCIAL EQUIPMENT SPECIFICATIONS

A. JTAG

Signal Name	Virtex-II™ Pin #	J1 JTAG Connection Pin #	Description
TDI	C2	7	Data Input
TCK	A15	4	Clock Input
TMS	B14	9	Test Mode Input
TDO	C15	6	Data Output

Table 6 JTAG Signal Descriptions

[From Ref 16]

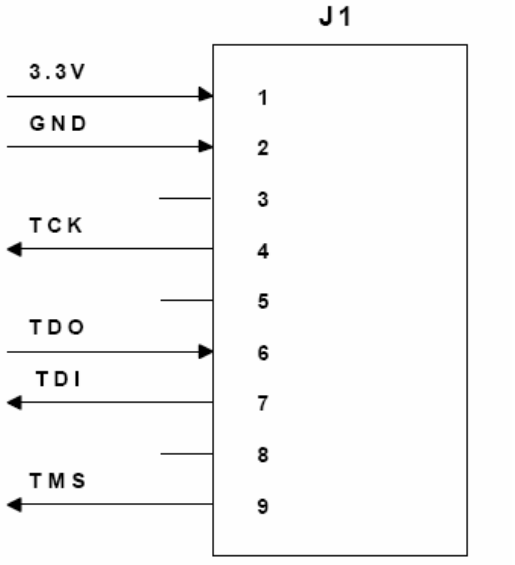


Figure 57 JTAG Connection Diagram

[From Ref 16]

B. POWER ELECTRONIC TEACHING SYSTEM DESCRIPTION

!NEW!

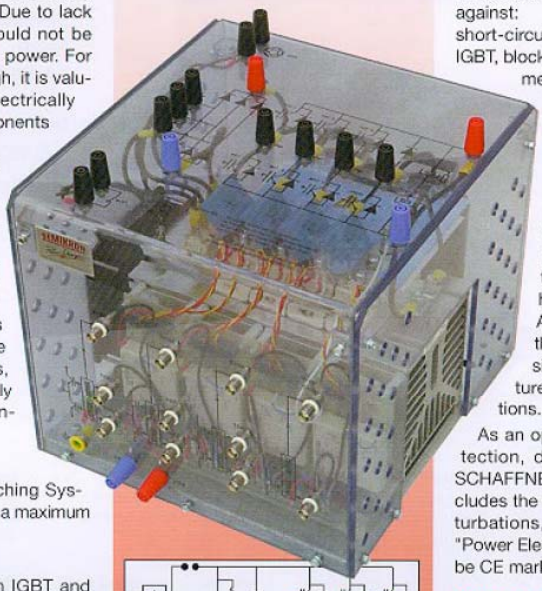
SEMIKRON
innovation+service

Power Electronics Teaching System

IGBT demonstration converter for schools and universities

When teaching and demonstrating the exciting world of power electronics , safety must be the main concern. Due to lack of experience, students should not be exposed immediately to live power. For a better understanding though, it is valuable to actually see and electrically access the individual components of the system.
The new "Power Electronics Teaching System" from SEMIKRON achieves exactly this.

The "Power Electronics Teaching System" will meet various application requirements regarding converters up to 20 kVA : 3 or 1 phase motors, DC current motors, UPS, active filter... or the totally new application you just invented!



Power Design

The "Power Electronics Teaching System" was designed to provide a maximum of 30 A rms per phase.

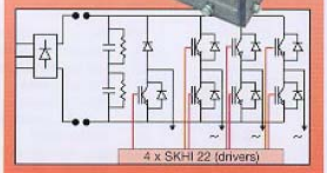
Major components:

- 3 half-bridges module with IGBT and CAL-diode SKM 50GB123D
  1 IGBT brake chopper SKM 50GAL123D
- a 3-phase diode rectifier SKD 51/14
- DC busbar capacitance of 1100 µF/ 800 V
- 4 SKHI 22 drivers

Output power capability: up to 20 kVA (3 phase)
Switching frequency: up to 20 kHz
Max input AC voltage : 3x480 V~ (400V with filter)

Passive Security

The power converter is protected by a plastic case on which all the standard security connectors for power ("banana" type) and command (BNC type) are fixed. This case offers double IP protection.



enables practical demonstrations and makes your projects safer and more efficient

makes the power electronics courses safe and prevents dangerous and expensive failures in your equipment

increases your demonstration time by reducing build-up time

Active Security

The driver SKHI 22 protects the IGBTs against:
short-circuits (detection, switch off the IGBT, blocking of all further signals, error message)
under-voltage of the power supply (blocking of all signals, error message), simultaneous command of both IGBTs in one phase-leg (through logic and dead-time).
Furthermore, a thermal protection prohibits destructive heatsink temperatures.
A sensor has been placed at the warmest point of the heatsink to measure the temperature and validate your calculations.

As an option, a complete EMC protection, defined in partnership with SCHAFFNER, can be delivered. This includes the filter against conducted perturbations, this protection allows the "Power Electronics Teaching System" to be CE marked.

Applications Manual/ initial class assignments

With over 40 years of experience SEMIKRON has designed its "Power Electronics Teaching System" to expose students to realistic industrial applications design. The manual also gives an example for an initial educational demonstration. Students can compare the test results with the calculation method in the manual.

SEMIKRON Quality

As a leader in power IGBT power systems, SEMIKRON ensures the quality of your "Power Electronics Teaching System" by providing a final test certificate. Every IGBT of each power stack is tested in short-circuit, at maximum voltage, and the complete stack is tested under full load conditions (max. current, max. DC Voltage).

marketing info + marketing info + marketing info + marketing info + marketing info + marketing info

C. MEMEC™ DEVELOPMENT KIT

Memec Design

Virtex™-II LC1000 Development Kit

Product Brief

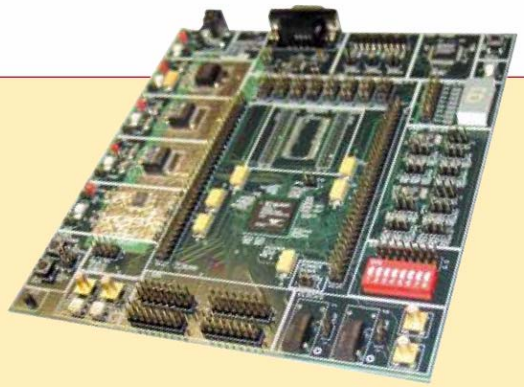
The Virtex-II LC1000 Development Kit verifies platform FPGA design applications.

Features

- Easy to use development platform
- Based on the Xilinx® 1 M gate Virtex-II FPGA (XC2V1000)
- User I/O expansion connectors
- Bank selectable reference voltage and resistors to support multiple I/O standards
- Supports four clock inputs
- Two user clock outputs via SMB connectors
- High performance 32 MB DDR memory
- LVDS transmit and receive ports
- Low cost and high flexibility

Applications

- General-purpose prototyping platform
- Digital signal processing
- Telecommunication and networking
- Video and wireless



Product Description

The Virtex-II LC1000 Development Kit provides an easy to use development platform for prototyping and verifying Virtex-II based designs. The Virtex-II family is a platform FPGA intended for high performance, low to high-density designs with IP cores and customized modules. The Virtex-II family delivers complete solutions for telecommunication, wireless, networking, video, and DSP applications. In addition to performance and density, the Virtex-II family offers many supported I/O standards, external interfaces for PCI-X, QDR and DDR, abundant memory resources and on-chip multipliers, features that enable FPGA designers to meet the design requirements of next generation telecommunication and networking applications. The Virtex-II reference board employs the Xilinx 1 M gate Virtex-II (XC2V1000) device. The reference board's supporting devices work in conjunction with the Xilinx Virtex-II FPGA to facilitate the prototype of high-performance memory and I/O interfaces such as differential signaling (LVDS) and high-speed DDR memory interfaces.

Virtex-II also includes a high performance and flexible digital clock manager (DCM) with on-chip digital controlled impedance (DCI) for source/load terminations, a feature that enables FPGA designers to perform high-level integration, reduce board level cost, and improve overall system level reliability and performance. The Virtex-II reference board provides the required test circuits for exploring and testing these functions. Advanced features such as in-system programmability of the on-board ISP PROM, complete high-performance differential signaling support, and the Reference Design Center's pre-configured reference designs make the kit a perfect solution for FPGA and system designers who need a quick, flexible and low cost prototyping platform.

The Virtex-II reference board utilizes the Xilinx XC18V04 ISP PROM, allowing FPGA designers to quickly download revisions and verify design changes so that they can meet the final system-level design requirements. In addition to the ISP PROM, the reference board provides a JTAG connector for direct configuration of the Virtex-II FPGA.

The Virtex-II reference board is bundled with VHDL and Verilog HDL reference design examples to help FPGA designers shorten development time and meet time-to-market requirements.

Virtex™-II LC1000 Development Kit

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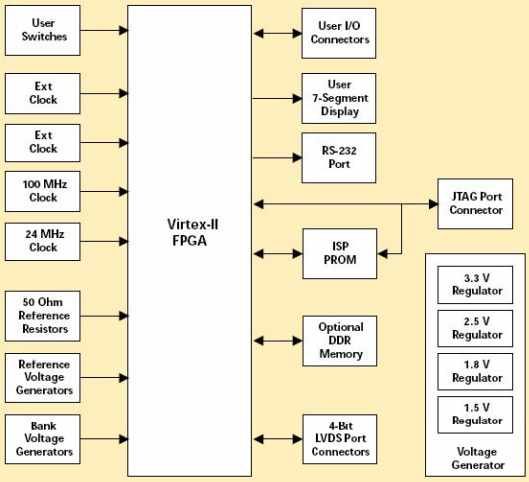
Contact Memec: xilinx.info@memecdesign.com 888.488.4133 x212 (North America Only) or 858.314.8190 (Outside US)

Memec Design

Virtex-II LC1000 Development Kit Includes:

- Virtex-II Reference Board
  - 1 M gate Virtex-II FPGA device (XC2V1000-4FG256C)
  - 3.3 V, 2.5 V, 1.8 V and 1.5 V on-board voltage regulators
  - XC18V04 ISP PROM
  - On-board 32 MB DDR memory
  - RS-232 port
  - User switches and user I/O ports
  - Seven-segment LED display
  - LVDS transmit and receive ports
  - Eight-bank SelectI/O voltage (VCCO) settings (1.5 V, 1.8 V, 2.5 V and 3.3 V options)
  - Eight-bank reference voltage (VREF) settings (1.5 V, 1.25 V, 1.0 V, 0.90 V and 0.75 V options)
  - Bank reference resistors to support DCI
  - Two on-board clock sources and two SMB user clock inputs
  - Two user SMB clock output connectors
  - JTAG port
- AC-to-DC power supply adapter
- Complete reference designs with source code (VHDL and Verilog HDL)
- Bundled software options



Ordering Information

	Americas Part #	International Part #
Virtex-II LC1000 Development Kit		
Virtex-II Development Kit	DS-KIT-V2LC1000	DS-KIT-V2LC1000-EURO
Kit with ISE Alliance and JTAG Cable	DS-KIT-V2LC1000-ALI	
Kit with ISE Foundation and JTAG Cable	DS-KIT-V2LC1000-ISE	

Virtex™-II LC1000 Development Kit

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